Device Features

BlueCore™4-Flash Plug-n-Go™

- Fully Qualified Bluetooth v2.0+EDR
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Low Power 1.8V operation
- 10 x 10mm 96-ball LFBGA Package
- Minimum External Components
- Integrated 1.8V Regulator
- Dual UART Ports
- RF Plug-n-Go Package
- 50Ω Matched Connection to Antenna
- RoHS Compliant

Single Chip Bluetooth®

v2.0 + EDR System

Advance Information Data Sheet For

BC419143B

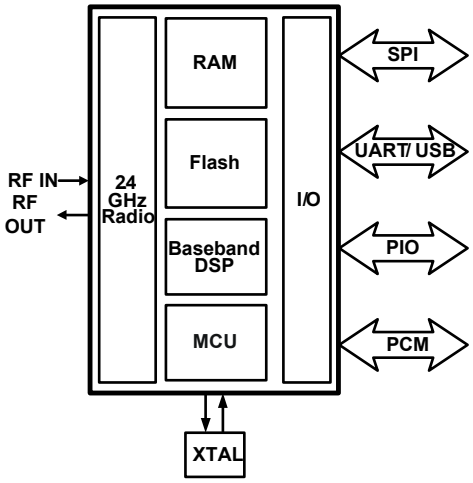
April 2006

General Description

The **BlueCore™4-Flash Plug-n-Go™** is a single chip radio and baseband IC for Bluetooth 2.4GHz systems. It is implemented in 0.18µm CMOS technology.

BC419143B contains 8Mbit of internal Flash memory. When used with CSR Bluetooth stack, it provides a fully compliant Bluetooth system to v2.0 + EDR of the specification for data and voice.

BlueCore4-Flash Plug-n-Go has the same pinout and electrical characteristics as available in BlueCore4-ROM Plug-n-Go to enable development of custom code before committing to ROM. It also has the same pinout as BlueCore2-ROM Plug-n-Go and BlueCore2-Flash Plug-n-Go to keep compatibility.



System Architecture

Applications

- Automotive

BlueCore4-Flash Plug-n-Go has been designed to reduce the number of external components required which ensures production costs are minimised. The 0.8mm pitch BlueCore4-Flash Plug-n-Go can be used on either two or four layer PCB construction.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.0 + EDR specification.

BlueCore™4-Flash Plug-n-Go™ Data Sheet

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1 Status Information

The status of this Data Sheet is **Advance Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

RoHS Compliance

BlueCore4-Flash Plug-n-Go devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

2 Key Features

Radio

- Direct 50Ω connection to a common TX/RX antenna
- Bluetooth v2.0+EDR specification compliant
- Extensive built-in self-test minimises production test time
- No external trimming is required in production
- Antenna matching and filtering within IC

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low Park/Sniff/Hold mode
- Clock request output to control external clock
- On-chip linear regulator, producing 1.8V output from 2.2V to 4.2V input
- Power on reset cell detects low supply voltage
- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to application

Baseband and Software

- Internal programmed 8Mbit flash for complete system solution
- 48kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full seven slave piconet operation
- Logic for forward error correction, header error control, access code correlation, demodulation, CRC, encryption bitstream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4M baud for system debugging
- UART interface with programmable baud rate up to 3M baud with an optional bypass mode
- Full speed USB interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0
- Synchronous bi-directional serial programmable audio interface
- Optional I²C™ compatible interface

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customer specific builds with embedded application code

Package Options

- 96-ball LFBGA 10 x 10 x 1.6mm 0.8mm pitch

3 Package Information

3.1 BC419143B Pinout Diagram

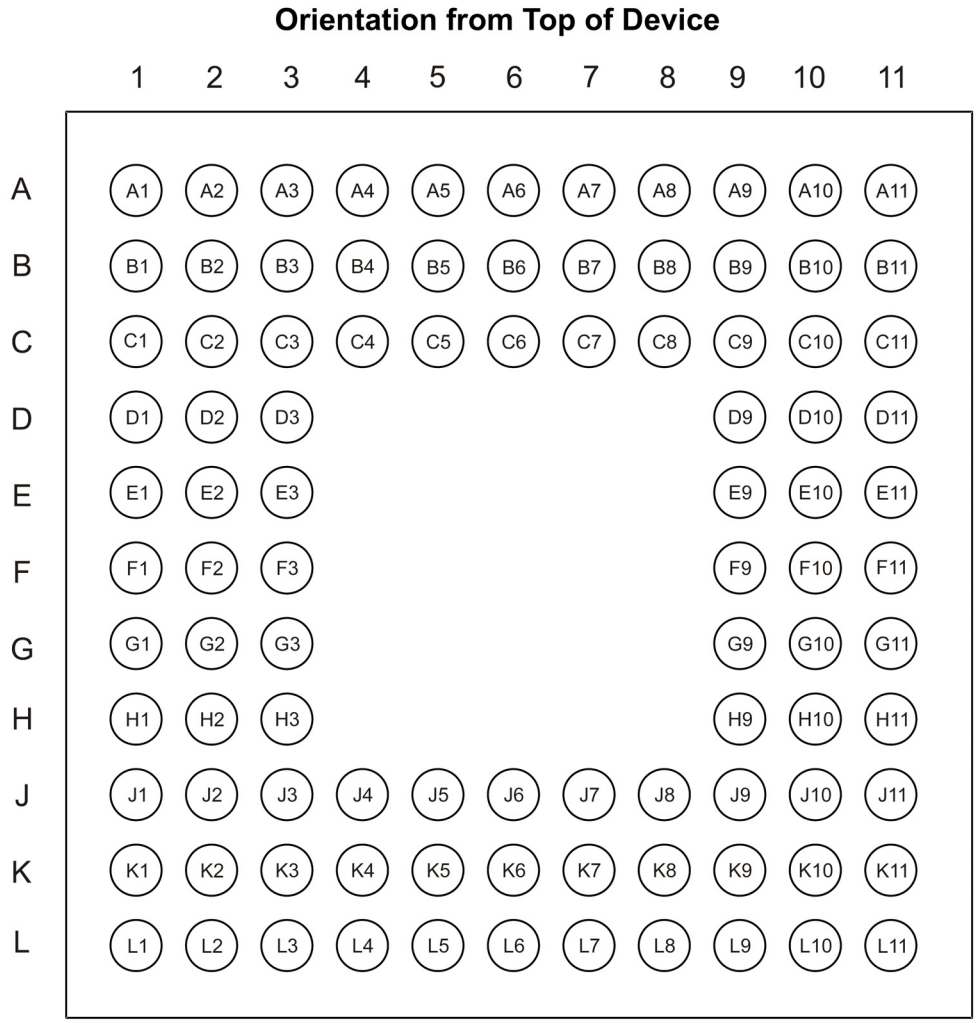


Figure 3.1: BlueCore4-Flash Plug-n-Go 10 x 10mm LFBGA Package

3.2 BC419143B-ANN-E4 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D2	Analogue	Single ended receiver input
PIO[0]/RXEN	D3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[1]/TXEN	C4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
BAL_MATCH	A1	Analogue	Tie to VSS_RADIO
RF_CONNECT	B1	Analogue	50Ω RF matched I/O
AUX_DAC	C2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L3	Analogue	For crystal or external clock input
XTAL_OUT	L4	Analogue	Drive for crystal

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G10	CMOS output, tristatable with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tri-state with weak internal pull-up	UART data output active low
UART_RX	J11	CMOS input with weak internal pull-down	UART data input active low (idle status high)
UART_RTS	L11	CMOS output, tristatable with weak internal pull-up	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	L9	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L8	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESET	F9	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESETB	G9	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C10	CMOS input with weak internal pull-up	Chip select for Serial Peripheral Interface, active low
SPI_CLK	D10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	D11	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	C11	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	E9	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)
FLASH_EN	B10	No Connect	Not available for BlueCore4-Flash Plug-n-Go

PIO Port	Ball	Pad Type	Description
PIO[2]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	B2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	H9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	J8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	K8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	K9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	A4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	A5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	K5	Bi-directional	Programmable input/output line
AIO[1]	J6	Bi-directional	Programmable input/output line
AIO[2]	K7	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	L7	Regulator input	Linear regulator voltage input
VREG_EN	J2	Digital input	Active high, regulator enable pin with internal pull-up
VDD_USB	L10	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC[a]
VDD_PADS	E11	VDD	Positive supply for all other digital input/output ports[b]
VDD_DIG	L6	Regulator output	Positive 1.8V supply output for VDD_MEM and VDD_CORE
VDD_MEM	B11, K6	VDD	Positive supply for internal memory and AIO ports
VDD_CORE	F11	VDD	Positive supply for internal digital circuitry
VDD_RADIO	E3	VDD	Positive supply for RF circuitry
VDD_ANA	L5	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VDD_BALUN	F1	VDD	Positive supply for balun
VSS_PADS	A2, E10, K10	VSS	Ground connection for input/output
VSS_MEM	D9, J9	VSS	Ground connections for AIO and Extended PIO ports
VSS_CORE	F10	VSS	Ground connection for internal digital circuitry
VSS_RADIO	E2, F3, G2	VSS	Ground connections for RF circuitry
VSS_VCO	G3, H2 H3	VSS	Ground connections for VCO and synthesiser
VSS_ANA	K4	VSS	Ground connection for analogue circuitry
VSS_BALUN	G1,J1, K1	VSS	Ground connection for balun

(a) Positive supply for PIO[3:0] and PIO[11:8]
(b) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
N/C	A6, A7, A8, A9, A10, A11, B5, B6, B7, B8, B9, C1, C5, C6, C7, C8, C9, D1, E1, F2, H1, J3, J4, J5, J7, K2, K3, L1, L2	Leave unconnected

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	+125°C
Supply Voltage: VDD_MEM, VDD_RADIO, VDD_ANA, VDD_BAL and VDD_CORE	-0.4V	2.2V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature Range	-40°C	+85°C
Guaranteed RF performance range (a)	-25°C	+85°C
Supply Voltage: VDD_MEM, VDD_RADIO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN	2.2V	4.2V(b)

(a) Typical figures are given for RF performance between -40°C and +85°C.

(b) The device will operate without damage with VREG_IN as high as 5.6V, however the RF performance is not guaranteed above 4.2V.

Input/Output Terminal Characteristics (Supply)				
Linear Regulator	**Min**	**Typ**	**Max**	**Unit**
Normal Operation				
Output Voltage[a] (I_{load} = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[b] [c]	-	-	1	mV rms
Load Regulation (I_{load} < 100 mA)	-	-	50	mV/A
Settling Time[b] [d]	-	-	50	µs
Maximum Output Current	140	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	4.2[e]	V
Dropout Voltage (I_{load} = 70 mA)	-	-	350	mV
Quiescent Current (excluding load, I_{load} < 1mA)	25	35	50	µA
Low Power Mode[f]				
Quiescent Current (excluding load, I_{load} < 100µA)	4	7	10	µA
Disabled Mode[g]				
Quiescent Current	1.5	2.5	3.5	µA

(a) For optimum performance, the VDD_ANA ball adjacent to VREG_IN should be used for regulator output,

(b) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(c) Frequency range is 100Hz to 100kHz.

(d) 1mA to 70mA pulsed load.

(e) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore4-Flash Plug-n-Go, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V.

(f) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(g) Regulator is disabled when VREG_EN is pulled low. It is also disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA.

Input/Output Terminal Characteristics (Digital)					
Digital Terminals		**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		+10	+40	+100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		+0.2	+1.0	+5.0	µA
I/O pad leakage current		-1	0	+1	µA
C_I Input Capacitance		1.0	-	5.0	pF

USB Terminals	**Min**	**Typ**	**Max**	**Unit**
VDD_USB for correct USB operation	3.1		3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V
Input Leakage Current				
VSS_PADS < VIN < VDD_USB[a]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

(a) Internal USB pull-up disabled

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[a]		-	-	700	Samples/s

[a] ADC is accessed through the VM function. The sample rate given is achieved as part of this function.

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size[a]	12.5	14.5	17.0	mV
Output Voltage		monotonic[a]		
Voltage range (I_O=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non-linearity[a]	-2	-	2	LSB
Settling time (50pF load)	-	-	10	µs

[a] Specified for an output voltage between 0.2V and VDD_PIO -0.2V. Output is high impedance when chip is in Deep Sleep mode.

Crystal Oscillator	Min	Typ	Max	Unit
Crystal frequency[a]	8.0	-	32.0	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
External Clock				
Input frequency[d]	7.5	-	40.0	MHz
Clock input level[e]	0.2	-	VDD_ANA	V pk-pk
Allowable Jitter	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	kΩ
XTAL_IN input capacitance	-	7	-	pF

(a) Integer multiple of 250kHz

(b) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

(c) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF.

(d) Clock input can be any frequency between 8MHz and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

(e) Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

4.1 Power Consumption

Typical Average Current Consumption		
VDD=1.8V **Temperature = +20°C**	**Output Power = +4dBm**	
Mode	**Average**	**Unit**
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	21	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	21	mA
SCO connection HV3 (No Sniff Mode) (Slave)	28	mA
SCO connection HV1 (Slave)	42	mA
SCO connection HV1 (Master)	42	mA
ACL data transfer 115.2kbps UART no traffic (Master)	5	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	22	mA
ACL data transfer 720kbps UART (Master or Slave)	45	mA
ACL data transfer 720kbps USB (Master or Slave)	45	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	3.2	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.45	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.55	mA
Standby Mode (Connected to host, no RF activity)	47.0	µA
Reset (RESET high or RESETB low)	15.0	µA

Typical Peak Current at +20°C	
Device Activity/State	**Current (mA)**
Peak Current during cold boot (100ms sampling interval)	-
Peak TX Current Average across burst)	-
Peak RX Current	-
Average RX Current across burst	-

Conditions	
VREG_IN, VDD_PIO, VDD_PADS	-
Host Interface	-
Baud Rate	-
Clock Source	-
Output Power	-
Receive Sensitivity	-
Device Mode	-
Packet Type	-

5 Radio Characteristics - Basic Data Rate

5.1 Temperature +20°C

5.1.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +20°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power(a) (b)	-	2.5	-	-6 to +4(c)	dBm
RF power variation over temperature range with compensation enabled(±)(d)	-	1.5	-	-	dB
RF power variation over temperature range with compensation disabled(±)(d)	-	2.5	-	-	dB
RF power control range	-	35	-	≥16	dB
RF power range control resolution(e)	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$(f) (g)	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$(f) (g)	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F = F_0 \pm > 3MHz$(f) (g)	-	-50	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	165	-	$140<f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	150	-	115	kHz
$\Delta f1_{avg}/\Delta f2_{avg}$	-	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz
2nd Harmonic Content	-	TBD	-	≤-30	dBm
3rd Harmonic Content	-	TBD	-	≤-30	dBm

(a) The BlueCore4-Flash Plug-n-Go firmware maintains the transmit power within Bluetooth v2.0+EDR specification limits

(b) Measurement using PSKEY_LC_MAX_TX_POWER setting corresponding to a PSKEY_LC_POWER_TABLE power table entry = 63

(c) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(d) These parameters are dependent on matching circuit used, and its behaviour over temperature, therefore these parameters are not under CSR's direct control

(e) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level > 20

(f) Measured at F_0 = 2441MHz

(g) BlueCore4-Flash Plug-n-Go guaranteed to meet ACP performance in Bluetooth v2.0+EDR specification, three exceptions allowed.

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Emitted power in cellular bands measured at unbalanced port of the balun. Output power = TBDdBm	0.869 - 0.894[a]	-	TBD	-	GSM 850	dBm / Hz
	0.869 - 0.894[b]	-	TBD	-	CDMA 850	
	0.925 - 0.960[a]	-	TBD	-	GSM 900	
	1.570 - 1.580[c]	-	TBD	-	GPS	
	1.805 - 1.880[a]	-	TBD	-	GSM 1800 / DCS 1800	
	1.930 - 1.990[d]	-	TBD	-	PCS 1900	
	1.930 - 1.990[b]	-	TBD	-	GSM 1900	
	1.930 - 1.990[a]	-	TBD	-	CDMA 1900	
	2.110 - 2.170[b]	-	TBD	-	W-CDMA 2000	
	2.110 - 2.170[e]	-	TBD	-	W-CDMA 2000	

(a) Integrated in 200kHz bandwidth and then normalised to 1Hz bandwidth
(b) Integrated in 1.2MHz bandwidth and then normalised to 1Hz bandwidth
(c) Integrated in 1MHz bandwidth and then normalised to 1Hz bandwidth
(d) Integrated in 30kHz bandwidth and then normalised to 1Hz bandwidth
(e) Integrated in 5MHz bandwidth and then normalised to 1Hz bandwidth

5.1.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +20°C		
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-85.0	-	≤70	dBm
	2.441	-	-85.0	-		
	2.480	-	-87.0	-		
Maximum received signal at 0.1% BER		-	0	-	≥20	dBm
	Frequency (MHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Continuous power required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	30-2000	-	0	-	-10	dBm
	2000-2400	-	0	-	-27	
	2500-3000	-	0	-	-27	
C/I co-channel		-	6	-	≤11	dB
Adjacent channel selectivity C/I $F = F_0 + 1MHz$ (a) (b)		-	-5	-	≤0	dB
Adjacent channel selectivity C/I $F = F_0 - 1MHz$ (a) (b)		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F = F_0 + 2MHz$ (a) (b)		-	-38	-	≤-30	dB
Adjacent channel selectivity C/I $F = F_0 - 2MHz$ (a) (b)		-	-23	-	≤-20	dB
Adjacent channel selectivity C/I $F = F_0 + 3MHz$ (a) (b)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F = F_0 - 5MHz$ (a) (b)		-	-44	-	≤-40	dB
Adjacent channel selectivity C/I $F = F_{Image}$ (a) (b)		-	-22	-	≤-9	dB
Maximum level of intermodulation interferers (c)		-	TBD	-	≤-39	dBm
Spurious output level (d)		-	TBD	-	-	dBm/Hz

(a) Up to five exceptions are allowed in v2.0+EDR of the Bluetooth specification. BlueCore4-Flash Plug-n-Go is guaranteed to meet the C/I performance as specified by the Bluetooth specification v2.0+EDR.

(b) Measured at F = 2441MHz

(c) Measured at f1 - f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c., i.e., wanted signal at -64dBm.

(d) Measured at unbalanced port of the balun. Integrated in 100kHz bandwidth and normalised to 1Hz. Actual figure is typically below -150dBm/Hz except for peaks of -70dbm at 1600MHz, -60dBm inband at 2.4GHz and -70dBm at 3.2GHz.

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Continuous power in cellular bands required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at unbalanced port of the balun.	0.824 - 0.849	-	0	-	GSM 850	dBm
	0.824 - 0.849	-	-10	-	CDMA 850	
	0.880 - 0.915	-	-5	-	GSM 900	
	1.710 - 1.785	-	0	-	GSM 1800 / DCS 1800	
	1.850 - 1.910	-	0	-	GSM 1900 / PCS 1900	
	1.850 - 1.910	-	-7	-	CDMA 1900	
	1.920 - 1.980	-	-10	-	W-CDMA 2000	
Continuous power in cellular bands required to block Bluetooth reception (for input power of -72dBm with 0.1% BER) measured at unbalanced port of the balun.	0.824 - 0.849	-	-2	-	GSM 850	dBm
	0.824 - 0.849	-	-12	-	CDMA 850	
	0.880 - 0.915	-	-7	-	GSM 900	
	1.710 - 1.785	-	0	-	GSM 1800 / DCS 1800	
	1.850 - 1.910	-	0	-	GSM 1900 / PCS 1900	
	1.850 - 1.910	-	-12	-	CDMA 1900	
	1.920 - 1.980	-	-14	-	W-CDMA 2000	

5.2 Temperature -40°C

5.2.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = -40°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	3.5	-	-6 to +4[b]	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$	-	-45	-	≤-40	dBm
$\Delta f1_{avg}$ Maximum Modulation	-	165	-	$140<\Delta f1_{avg}<175$	kHz
$\Delta f2_{max}$ Minimum Modulation	-	151	-	115	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	-	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-	10	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	12	-	≤40	kHz

(a) BlueCore4-Flash Plug-n-Go firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits

(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification

(c) Measured at F_0 = 2441MHz

(d) Three exceptions are allowed in Bluetooth v2.0+EDR specification

5.2.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = -40°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-86	-	≤-70	dBm
	2.441	-	-86	-		
	2.480	-	-88	-		
Maximum received signal at 0.1% BER		-	TBD	-	≥-20	dBm

5.3 Temperature -25°C

5.3.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = -25°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	3.0	-	-6 to +4[b]	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-45	-	≤-40	dBm
$\Delta f1avg$ Maximum Modulation	-	165	-	140<$\Delta f1avg$<175	kHz
$\Delta f2max$ Minimum Modulation	-	151	-	115	kHz
$\Delta f2avg/\Delta f1avg$	-	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	12	-	≤40	kHz

(a) BlueCore4-Flash Plug-n-Go firmware maintains the transmit power to be within the Bluetooth specification v2.0+EDR limits.

(b) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(c) Measured at F_0 = 2441MHz

(d) Up to three exceptions are allowed in v2.0+EDR of the Bluetooth specification.

5.3.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = -25°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-86	-	≤-70	dBm
	2.441	-	-86	-		
	2.480	-	-87	-		
Maximum received signal at 0.1% BER		-	TBD	-	≥-20	dBm

5.4 Temperature +85°C

5.4.1 Transmitter

Radio Characteristics	VDD = 1.8V		Temperature = +85°C		
	Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]	-	0	-	-6 to +4[b]	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power $F = F_0 \pm 2MHz$[c] [d]	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F = F_0 \pm 3MHz$[c] [d]	-	-45	-	≤-40	dBm
$\Delta f1avg$ Maximum Modulation	-	165	-	140<$\Delta f1avg$<175	kHz
$\Delta f2max$ Minimum Modulation	-	148	-	115	kHz
$\Delta f2avg/\Delta f1avg$	-	0.97	-	≥0.80	-
Initial carrier frequency tolerance	-	7	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz

(a) BlueCore4-Flash Plug-n-Go firmware maintains the transmit power to be within the Bluetooth specification v2.0+EDR limits

(b) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR

(c) Measured at F_0 = 2441MHz

(d) Up to three exceptions are allowed in v2.0+EDR of the Bluetooth specification

5.4.2 Receiver

Radio Characteristics		VDD = 1.8V		Temperature = +85°C		
	Frequency (GHz)	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.1% BER for all packet types	2.402	-	-81	-	≤-70	dBm
	2.441	-	-81	-		
	2.480	-	-82	-		
Maximum received signal at 0.1% BER		-20	TBD	-	≥-20	dBm

6 Radio Characteristics - Enhanced Data Rate

6.1 Temperature +20°C

6.1.1 Transmitter

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	6	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1	-	-4 to +1	dB
Carrier frequency stability[c]		-	3	-	≤10	kHz
Modulation Accuracy[c] [d]	RMS DEVM	-	10	-	≤13[e]	%
	99% DEVM	-	15	-	≤20[e]	%
	Peak DEVM	-	20	-	≤25[e]	%

(a) BlueCore4-Flash Plug-n-Go firmware keeps RF transmit power within the Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurement methods are in accordance with the Bluetooth v2.0+EDR RF Test Specification
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
(e) The Bluetooth specification values are for 8DPSK modulation (values for the π/4 DQPSK modulation are less stringent)

Notes:

Results shown are referenced to the unbalanced port of the balun.

6.1.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +20°C				
	Modulation	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-86	-	≤-70	dBm
	8DPSK	-	-79	-	≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-6	-	≥-20	dBm
	8DPSK	-	-7	-	≥-20	dBm
C/I co-channel at 0.1% BER[a]	π/4 DQPSK	-	+11	-	≤+13	dB
	8DPSK	-	+19	-	≤+21	dB
Adjacent channel selectivity C/I $F=F_0$ +1MHz[a] [b] [c]	π/4 DQPSK	-	-8	-	≤0	dB
	8DPSK	-	-2	-	≤+5	dB
Adjacent channel selectivity C/I $F=F_0$ -1MHz [a] [b] [c]	π/4 DQPSK	-	-8	-	≤0	dB
	8DPSK	-	-2	-	≤+5	dB
Adjacent channel selectivity C/I $F=F_0$ +2MHz[a] [b] [c]	π/4 DQPSK	-	-35	-	≤-30	dB
	8DPSK	-	-35	-	≤-25	dB
Adjacent channel selectivity C/I $F=F_0$ -2MHz[a] [b] [c]	π/4 DQPSK	-	-23	-	≤-20	dB
	8DPSK	-	-19	-	≤-13	dB
Adjacent channel selectivity C/I $F \geq F_0$ +3MHz[a] [b] [c]	π/4 DQPSK	-	-43	-	≤-40	dB
	8DPSK	-	-40	-	≤-33	dB
Adjacent channel selectivity C/I $F \leq F_0$ 5MHz[a] [b] [c]	π/4 DQPSK	-	-43	-	≤-40	dB
	8DPSK	-	-38	-	≤-33	dB
Adjacent channel selectivity C/I $F=F_{Image}$[a] [b] [c]	π/4 DQPSK	-	-17	-	≤-7	dB
	8DPSK	-	-10	-	≤0	dB

(a) Measurements methods are in accordance with the Bluetooth v2.0+EDR RF Test Specification

(b) Up to five exceptions are allowed in the Bluetooth v2.0 +EDR RF Test Specification.BlueCore4-Flash Plug-n-Go is guaranteed to meet the C/I performance as specified by the Bluetooth v2.0 +EDR RF Test Specification

(c) Measured at F_0 = 2405MHz, 2441MHz, 2477MHz

Notes:

Results shown are referenced to the unbalanced port of the balun.

6.2 Temperature -40°C

6.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	8	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1	-	-4 to +1	dB
Carrier frequency stability[c]		-	3	-	≤10	kHz
Modulation Accuracy[c] [d]	RMS DEVM	-	10	-	≤13[e]	%
	99% DEVM	-	15	-	≤20[e]	%
	Peak DEVM	-	20	-	≤25[e]	%

(a) BlueCore4-Flash Plug-n-Go firmware keeps RF transmit power within the Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurements methods are in accordance with the Bluetooth v2.0+EDR RF Test specification
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
(e) The Bluetooth specification values are for 8DPSK modulation (values for the π/4 DQPSK modulation are less stringent)

Notes:

Results shown are referenced to the unbalanced port of the balun.

6.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-89	-	≤-70	dBm
	8DPSK	-	-82	-	≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-10	-	≥-20	dBm
	8DPSK	-	-10	-	≥-20	dBm

(a) Measurements methods are in accordance with the Bluetooth v2.0 + EDR RF Test Specification

Notes:

Results shown are referenced to the unbalanced port of the balun.

6.3 Temperature -25°C

6.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[a]		-	7	-	-6 to +4[b]	dBm
Relative transmit power[c]		-	-1	-	-4 to +1	dB
Carrier frequency stability[c]		-	3	-	≤10	kHz
Modulation Accuracy[c] [d]	RMS DEVM	-	10	-	≤13[e]	%
	99% DEVM	-	15	-	≤20[e]	%
	Peak DEVM	-	20	-	≤25[e]	%

(a) BlueCore4-Flash Plug-n-Go firmware keeps RF transmit power within the Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurement methods are in accordance with the Bluetooth v2.0+EDR RF Test Specification
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
(e) The Bluetooth specification values are for 8DPSK modulation (values for the π/4 DQPSK modulation are less stringent)

Notes:

Results shown are referenced to the unbalanced port of the balun.

6.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature =-25°C						
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER[a]	π/4 DQPSK	-	-87	-	≤-70	dBm
	8DPSK	-	-80	-	≤-70	dBm
Maximum received signal at 0.1% BER[a]	π/4 DQPSK	-	-10	-	≥-20	dBm
	8DPSK	-	-10	-	≥20	dBm

(a) Measurements methods are in accordance with the Bluetooth v2.0 +EDR RF Test Specification

Notes:

Results shown are referenced to the unbalanced port of the balun.

6.4 Temperature +85°C

6.4.1 Transmitter

Radio Characteristics	VDD = 1.8V	Temperature = +85°C				
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power (a)		-	1	-	-6 to +4(b)	dBm
Relative transmit power(c)		-	-1	-	-4 to +1	dB
Carrier frequency stability(c)		-	3	-	≤10	kHz
Modulation Accuracy(c) (d)	RMS DEVM	-	10	-	≤13(e)	%
	99% DEVM	-	15	-	≤20(e)	%
	Peak DEVM	-	20	-	≤25(e)	%

(a) BlueCore4-Flash Plug-n-Go firmware keeps RF transmit power within the Bluetooth v2.0+EDR specification limits
(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
(c) Measurement methods are in accordance with the Bluetooth v2.0 + EDR RF Test Specification
(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the carrier frequency drift.
(e) The Bluetooth specification values are for 8DPSK modulation (values for the π/4 DQPSK modulation are less stringent)

Notes:

Results shown are referenced to the unbalanced port of the balun.

6.4.2 Receiver

Radio Characteristics	VDD = 1.8V	Temperature = +85°C				
	Modulation	Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity at 0.01% BER(a)	π/4 DQPSK	-	-84	-	≤-70	dBm
	8DPSK	-	-77	-	≤-70	dBm
Maximum received signal at 0.1% BER(a)	π/4 DQPSK	-	0	-	≥-20	dBm
	8DPSK	-	-3	-	≥-20	dBm

(a) Measurements methods are in accordance with the Bluetooth v2.0 + EDR RF Test Specification

Notes:

Results shown are referenced to the unbalanced port of the balun.

7 Device Diagram

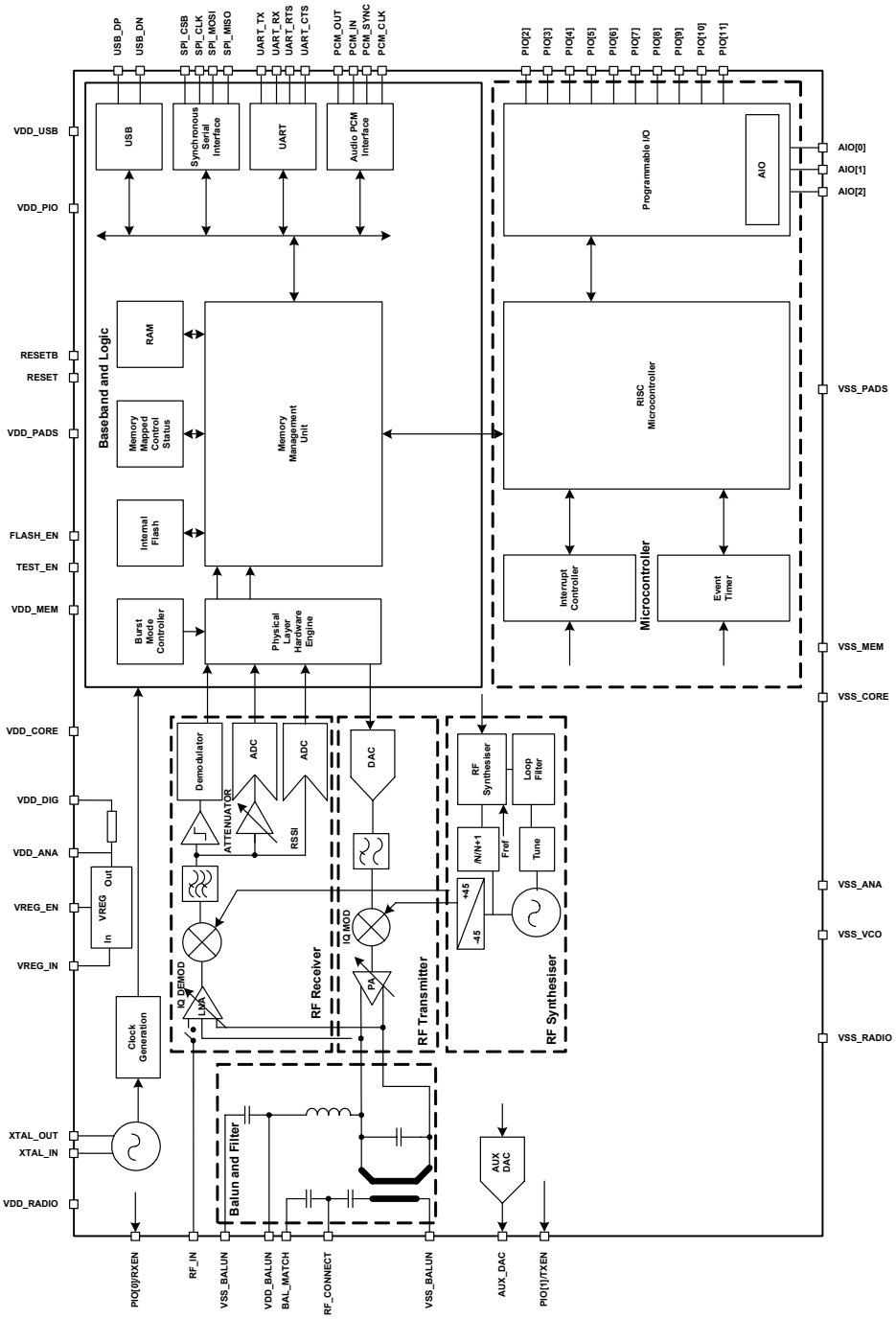


Figure 7.1: BlueCore4-Flash Plug-n-Go Device Diagram

8 Description of Functional Blocks

8.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-Flash Plug-n-Go to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an ADC is used to digitise the IF received signal.

8.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1[(1)] Bluetooth operation; differential mode is used for Class 2 operation.

8.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

8.2 RF Transmitter

8.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

8.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm. This allows BlueCore4-Flash Plug-n-Go to be used in Class 2 and Class 3 radios without an external RF PA.

8.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation or any other customer specific application.

8.3 Balun and Filter

The Plug-n-Go device incorporates a balun and filter to provide a 50Ω unbalanced antenna port.

8.4 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.0 + EDR specification.

8.5 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

8.6 Baseband and Logic

8.6.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

(1) Class 1 operation is not recommended for Plug-n-Go devices and therefore is not recommended for BlueCore4-Flash Plug-n-Go.

8.6.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

8.6.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware suports all optional and mandatory features of Bluetooth v2.0 + EDR including AFH and eSCO.

8.6.4 System RAM

48Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

8.6.5 Flash Memory (8Mbit)

8Mbits of internal Flash is available on the BC419143B. The Flash memory is provided for system firmware and the Kalimba DSP co-processor code implementation.

8.6.6 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore4-Flash Plug-n-Go acts as a USB peripheral, responding to requests from a master host controller such as a PC.

8.6.7 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

8.6.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

8.7 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

8.7.1 Programmable I/O

BlueCore4-Flash Plug-n-Go has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

8.7.2 802.11 Co-Existence Interface

Dedicated hardware is provided to implement a variety of co-existence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware. The details of some methods are proprietary (e.g., Intel WCS). Contact CSR for details.

9 CSR Bluetooth Software Stacks

BlueCore4-Flash Plug-n-Go is supplied with Bluetooth v2.0 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

The BlueCore4-Flash Plug-n-Go software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

9.1 BlueCore HCI Stack

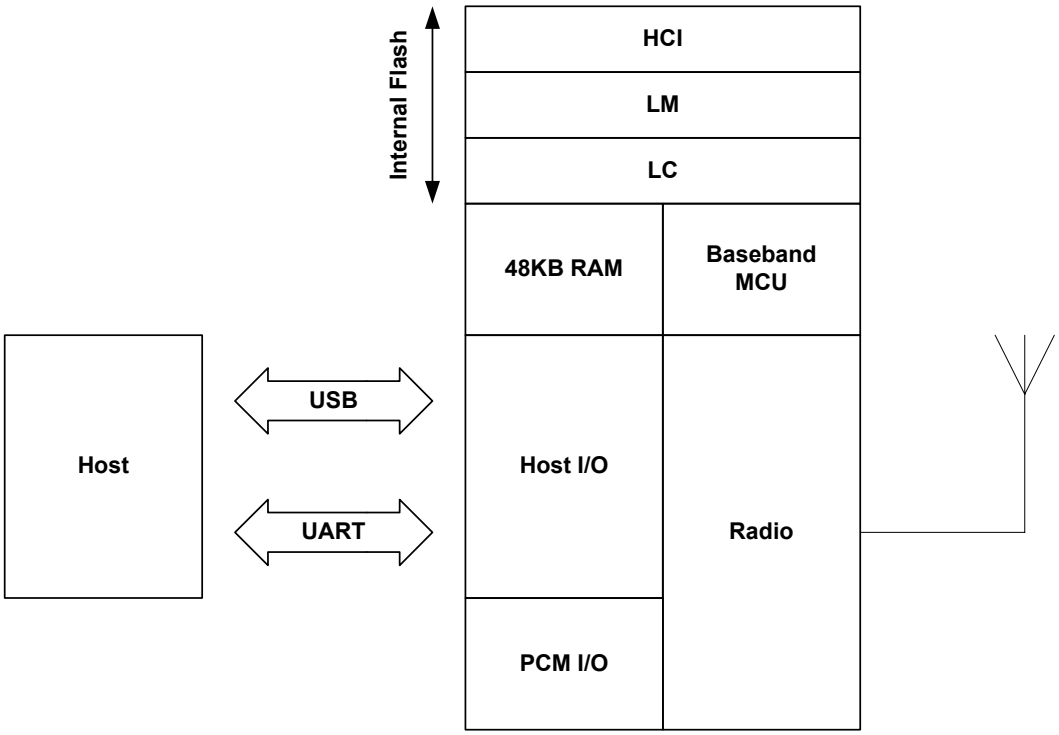


Figure 9.1: BlueCore HCI Stack

In the implementation shown in the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

9.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

Bluetooth v2.0 + EDR mandatory functionality:

- Adaptive frequency hopping (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- Adaptive Frequency Hopping (AFH) as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.0 + EDR specification.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps(1)
- Operation with up to seven active slaves(1)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csr.com.

(1) This is the maximum allowed by Bluetooth v2.0 + EDR specification.

(2) BlueCore4-Flash Plug-n-Go supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.0 + EDR specification.

9.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BlueCore Command (BCCMD), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART break condition can be used in three ways:
  1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  3. With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a Deep Sleep state.)
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of radio test or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

9.2 BlueCore RFCOMM Stack

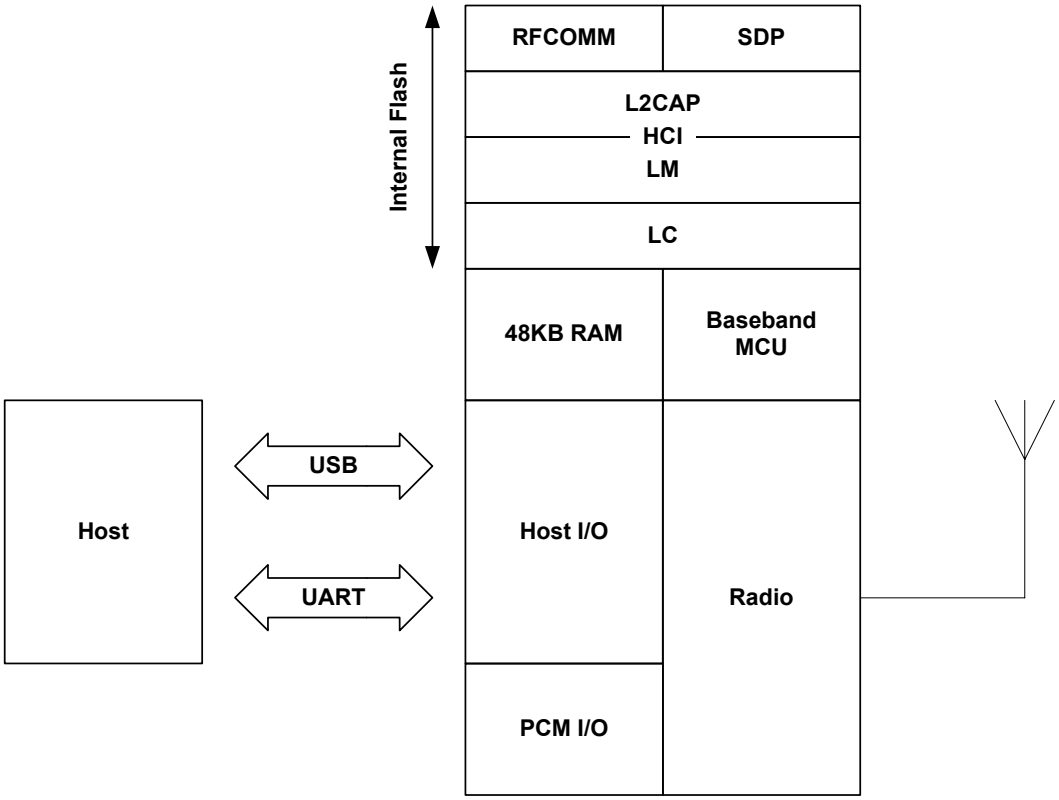


Figure 9.2: BlueCore RFCOMM Stack

In the version of the firmware, shown in Figure 9.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

9.2.1 Key Features of the RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: three
- Maximum number of simultaneous active ACL connections: three
- Maximum number of simultaneous active SCO connections: three
- Data Rate: up to 350kbps(1)

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

(1) The data rate is with respect to BlueCore4-Flash Plug-n-Go with basic data rate packets.

9.3 BlueCore Virtual Machine Stack

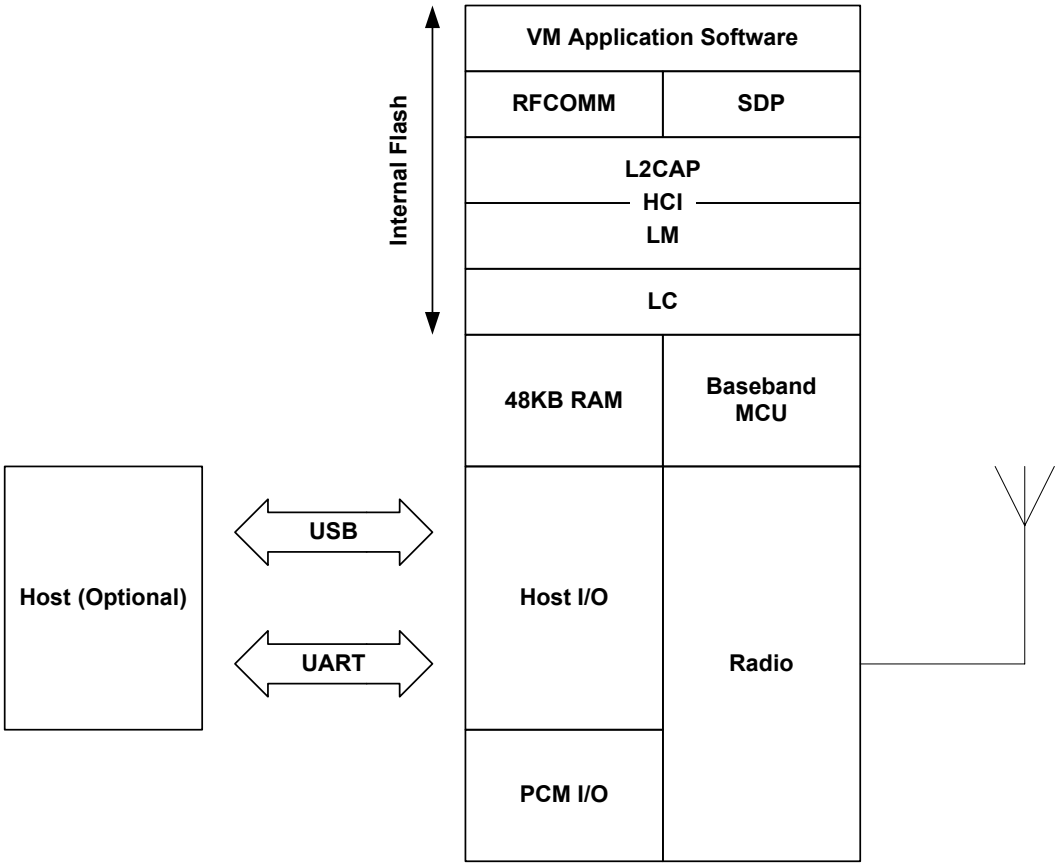


Figure 9.3: Virtual Machine

In Figure 9.3, this version of the stack firmware shown requires no host processor (but it can use a host processor for debugging, etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab SDK supplied with the BlueLab Multimedia and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless handsfree kit or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the handsfree profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

9.4 BlueCore HID Stack

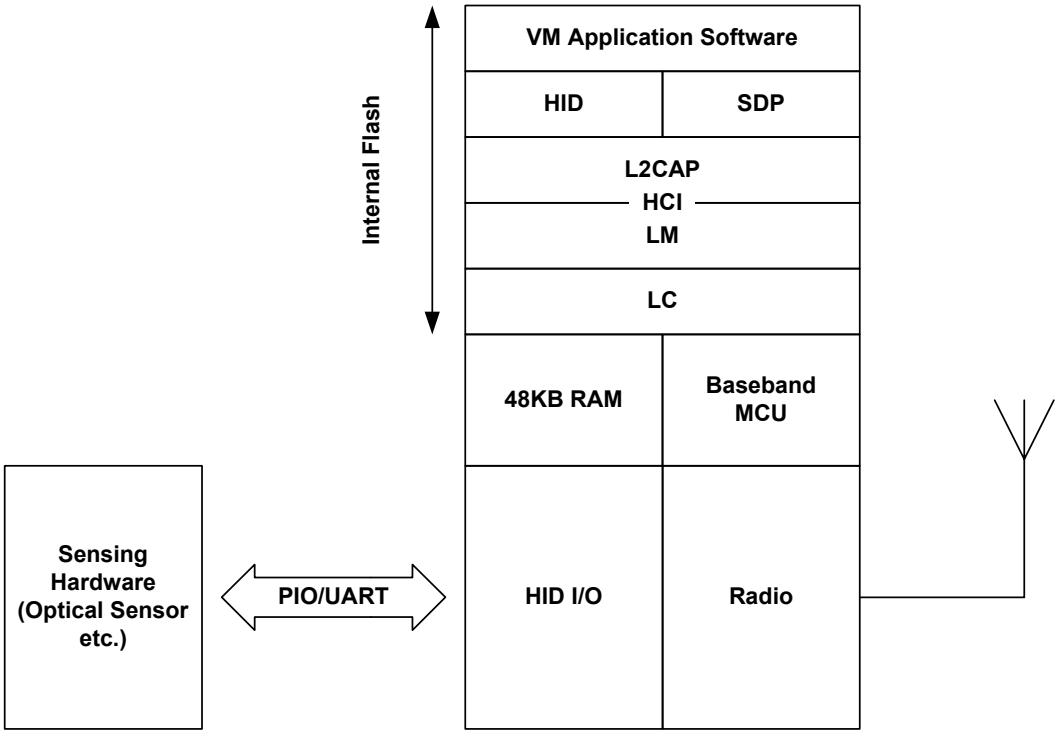


Figure 9.4: HID Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional SDK supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customise features such as power management and connect/reconnect behaviour.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include five mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available from CSR.

9.5 Host-Side Software

BlueCore4-Flash Plug-n-Go can be ordered with companion host-side software:

- BlueCore3-PC includes software for a full Windows 98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.
- BlueCore3-Mobile includes software for a full host-side stack designed for modern ARM chip-based mobile handsets together with IC hardware described in this document.

9.6 Device Firmware Upgrade

BlueCore4-Flash Plug-n-Go is supplied with boot loader software, which implements a Device Firmware Upgrade (DFU) capability. This allows new firmware to be uploaded to the Flash memory through BlueCore4-Flash Plug-n-Go UART or USB ports.

9.7 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, e.g., a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains three elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). BCHS also comes with example applications in ANSI C, which makes the process of writing the application easier.

9.8 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore4-Flash Plug-n-Go, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery Protocol (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

9.9 CSR Development Systems

CSR's BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore4-Flash Plug-n-Go hardware and software, and as toolkits for developing on-chip and host software.

10 Enhanced Data Rate

EDR has been introduced to provide 2x and 3x[1] data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore4-Flash Plug-n-Go supports both of the new data rates and is compliant with the Bluetooth v2.0+EDR specification.

10.1 Enhanced Data Rate Baseband

At the baseband level EDR utilises both the same 1.6kHz slot rate and the 1MHz symbol rate as defined for the basic data rate. Where EDR differs is that each symbol in the payload portion of a packet represents 2 or 3-bits. This is achieved using two new distinct modulation schemes. These are summarised in Table 10.1 and in Figure 10.1. Link Establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Data Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 10.1: Data Rate Schemes

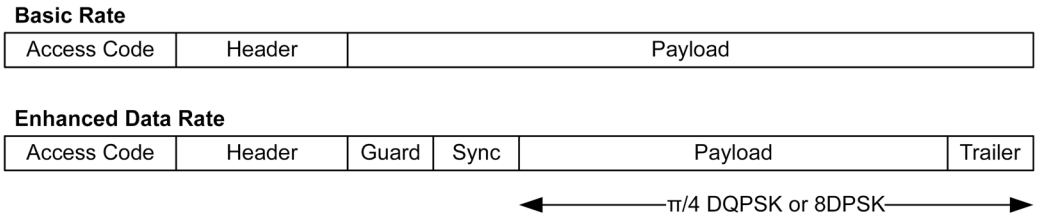


Figure 10.1: Basic Rate and Enhanced Data Rate Packet Structure

10.2 Enhanced Data Rate π/4 DQPSK

The 2x data rate for EDR utilises a π/4-DQPSK. Each symbol represents two bits of information. Figure 10.2 shows the constellation. It is described as having two planes, each having four points. Although it would appear that there are eight possible phase states, the encoding ensures that the trajectory of the modulation between symbols is restricted to the four states in the other plane.

For a given starting point, each phase change between symbols is restricted to +3π/4, +π/4, -π/4 or -3π/4 radians (+135°, +45°, -135° or -45°). For example, the arrows shown in Figure 10.2 represents trajectory to the four possible states in the other plane.Table 10.2 shows the phase shift encoding of symbols.

There are two primary advantages of utilising π/4-DQPSK modulation:

- The scheme avoids the crossing of the origin (a +π or -π phase shift) and therefore minimises amplitude variations in the envelope of the transmitted signal. This in turn allows the RF power amplifiers of the transmitter to be operated closer to their compression point without introducing spectral distortions. Consequently, the DC to RF efficiency is maximised.
- The differential encoding also allows for the demodulation without the knowledge of an absolute value for the phase of the RF carrier.

(1) The inclusion of 3x data rates is optional.

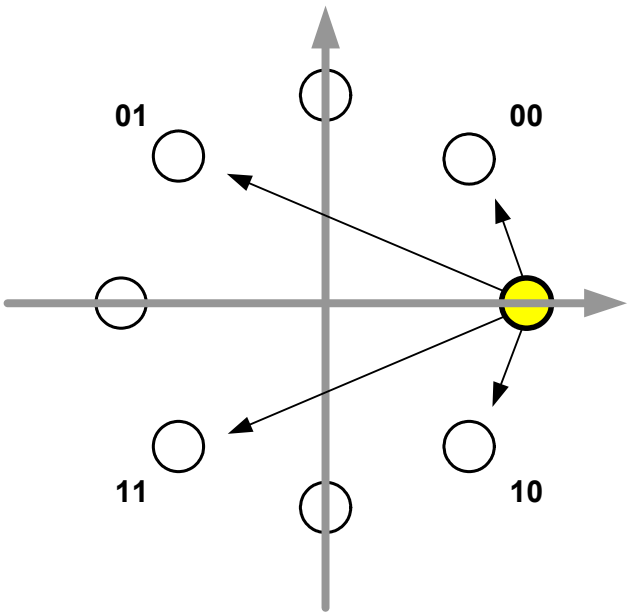


Figure 10.2: π/4 DQPSK Constellation Pattern

Bit Pattern	Phase Shift
00	π/4
01	3π/4
11	-3π/4
10	-π/4

Table 10.2: 2-Bits Determine Phase Shift Between Consecutive Symbols

10.3 Enhanced Data Rate 8DPSK

The 3x data rate modulation uses eight phase differential phase shift keying (8DPSK). Each symbol in the payload portion of the packet represents three baseband bits. Although it would appear that the 8DPSK is similar to π/4 DQPSK, the differential phase shifts between symbols are now permissible between any of the eight possible phase states. This reduces the separation between adjacent symbols on the constellation to π/4 (45°) and thereby reduces the noise and interference immunity of the modulation scheme. Nevertheless, since each symbol now represents 3 baseband bits, the actual throughput of the data is 3x when compared with the basic rate packet.

Figure 10.3 illustrates the 8DPSK constellation and Table 10.3 defines the phase encoding.

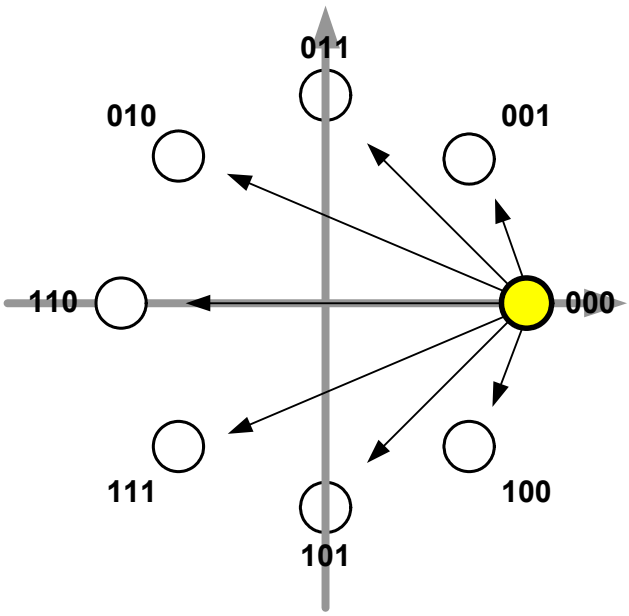


Figure 10.3: 8DPSK Constellation Pattern

Bit Pattern	Phase Shift
000	0
001	π/4
011	π/2
010	3π/4
110	π
111	-3π/4
101	-π/2
100	-π/4

Table 10.3: 3-Bits Determine Phase Shift Between Consecutive Symbols

11 Device Terminal Descriptions

11.1 RF Ports

The BlueCore4-Flash Plug-n-Go RF_IN terminal can be configured as either a single-ended or differential input. The operational mode is determined by setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x20).

11.1.1 RF Plug-n-Go

The package used on the BlueCore4-Flash Plug-n-Go device is an RF Plug-n-Go package, where the terminal RF_CONNECT forms an unbalanced ouput with a nominal 50Ω impedance. This terminal can be directly connected to an antenna requiring no impedance matching network as Figure 11.1 indicates.

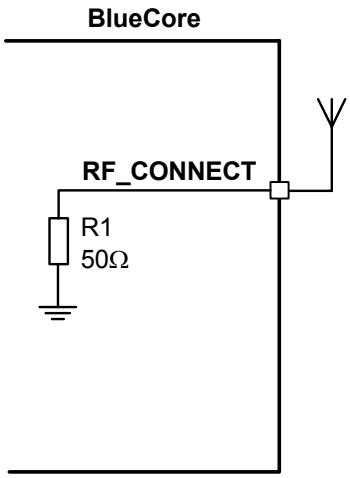


Figure 11.1: Circuit for RF_CONNECT

11.1.2 Single-Ended Input (RF_IN)

This is the single-ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

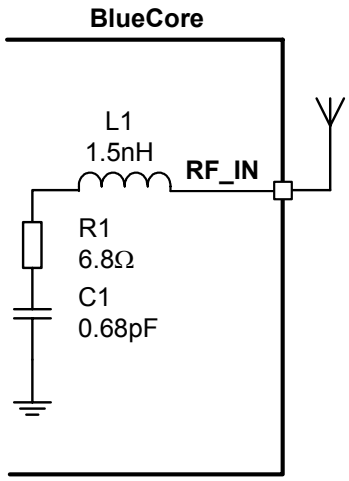


Figure 11.2: Circuit RF_IN

11.2 External Reference Clock Input (XTAL_IN)

The BlueCore4-Flash Plug-n-Go RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-Flash Plug-n-Go XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in section 11.3.

11.2.1 External Mode

BlueCore4-Flash Plug-n-Go can be configured to accept an external reference clock from another device (such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 11.1:

	Min	Typ	Max
Frequency[a]	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA[b] [c]

Table 11.1: External Clock Specifications

(a) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(b) VDD_ANA is 1.8V nominal

(c) If the external clock is driven through a DC blocking capacitor, then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk.

11.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from Deep Sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

11.2.3 Clock Timing Accuracy

As Figure 11.3 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.0 + EDR specification. Radio activity may occur after 11ms, therefore, at this point the timing accuracy of the external clock source must be within 20ppm.

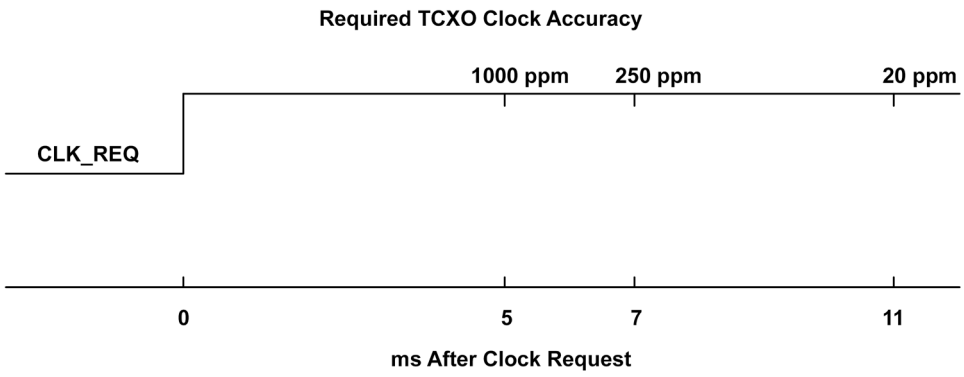


Figure 11.3: TCXO Clock Accuracy

11.2.4 Clock Start-Up Delay

BlueCore4-Flash Plug-n-Go hardware incorporates an automatic delay after the assertion of the system clock request signal before running firmware. By default, the delay is 5 low-power oscillator (LPO) cycles. At a nominal LPO frequency of 1 kHz, this equates to 5 ms. This is suitable for most applications using an external clock source.

However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-Flash Plug-n-Go provides a function that alters the system clock request signal to the period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is in units of LPO cycles from 1 to 31. Setting the key to zero gives a delay of 5 cycles, the default value.

The nominal frequency of the internal LPO is 1 kHz, however, the value varies somewhat between chips, so care should be taken to pick a suitable value. If an external slow clock at 32 kHz is supplied, this is divided by 32 before use.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-Flash Plug-n-Go as low as possible. BlueCore4-Flash Plug-n-Go consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

11.2.5 Input Frequencies and PS Key Settings

BlueCore4-Flash Plug-n-Go should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore4-Flash Plug-n-Go is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 11.2: PS Key Values for CDMA/3G Phone TCXO Frequencies

11.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

This section describes the crystal mode. See section 11.2 for the description of the external reference clock mode.

11.3.1 XTAL Mode

BlueCore4-Flash Plug-n-Go contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

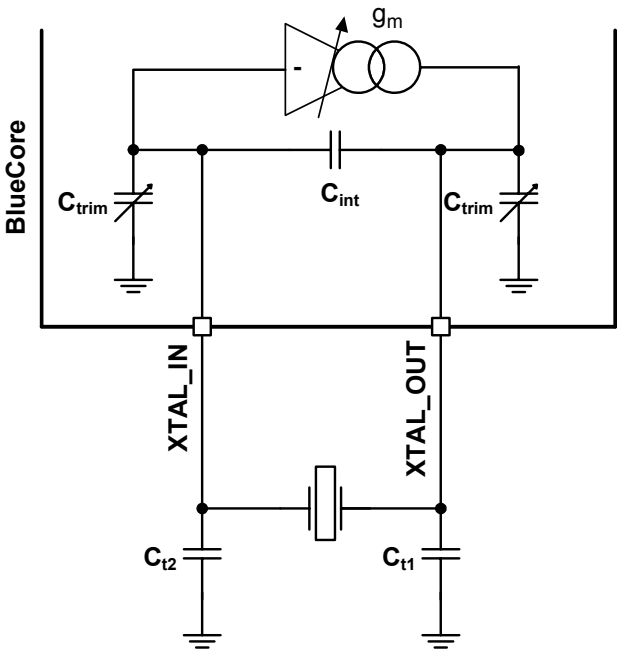


Figure 11.4: Crystal Driver Circuit

Figure 11.5 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

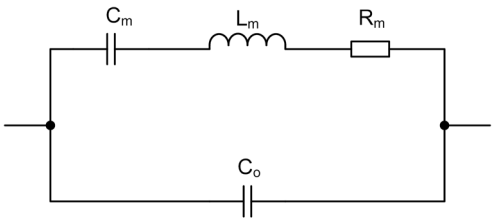


Figure 11.5: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore4-Flash Plug-n-Go contains variable internal capacitors to provide a fine trim.

	Min	Typ	Max
Frequency	8MHz	26MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 11.3: Crystal Specification

The BlueCore4-Flash Plug-n-Go driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

11.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-Flash Plug-n-Go provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence, slew rate at XTAL_IN (to which all on-chip clocks are referred). Crystal load capacitance, C_l is calculated with Equation 11.1:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \bullet C_{t2}}{C_{t1} + C_{t2}}$$

Equation 11.1: Load Capacitance

Where:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

11.3.3 Frequency Trim

BlueCore4-Flash Plug-n-Go enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the PS Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110fF \times PSKEY\_ANA\_FTRIM$$

Equation 11.2: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 11.3.

$$\frac{\Delta(F_X)}{F_X} = pullability \times 55 \times 10^{-3} (ppm/LSB)$$

Equation 11.3: Frequency Trim

Where Fx is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 11.4.

$$\frac{\partial(F_X)}{\partial(C)} = F_X \bullet \frac{C_m}{2(C_l + C_0)^2}$$

Equation 11.4: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 11.5.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

11.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-Flash Plug-n-Go uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 11.5:

$$g_m > \frac{3(2\pi F_x)^2 R_m((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}{(C_{t1} + C_{trim})(C_{t2} + C_{trim})}$$

Equation 11.5: Transconductance Required for Oscillation

BlueCore4-Flash Plug-n-Go guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance, by setting the PS Key PSKEY_XTAL_LVL (0x241).

11.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-Flash Plug-n-Go crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 11.6:

$$R_{neg} > \frac{(C_{t1} + C_{trim})(C_{t2} + C_{trim})}{g_m(2\pi F_X)^2((C_0 + C_{int})(C_{t1} + C_{t2} + 2C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}$$

Equation 11.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-Flash Plug-n-Go driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

11.3.6 Crystal PS Key Settings

See tables in section 11.2.5.

11.3.7 Crystal Oscillator Characteristics

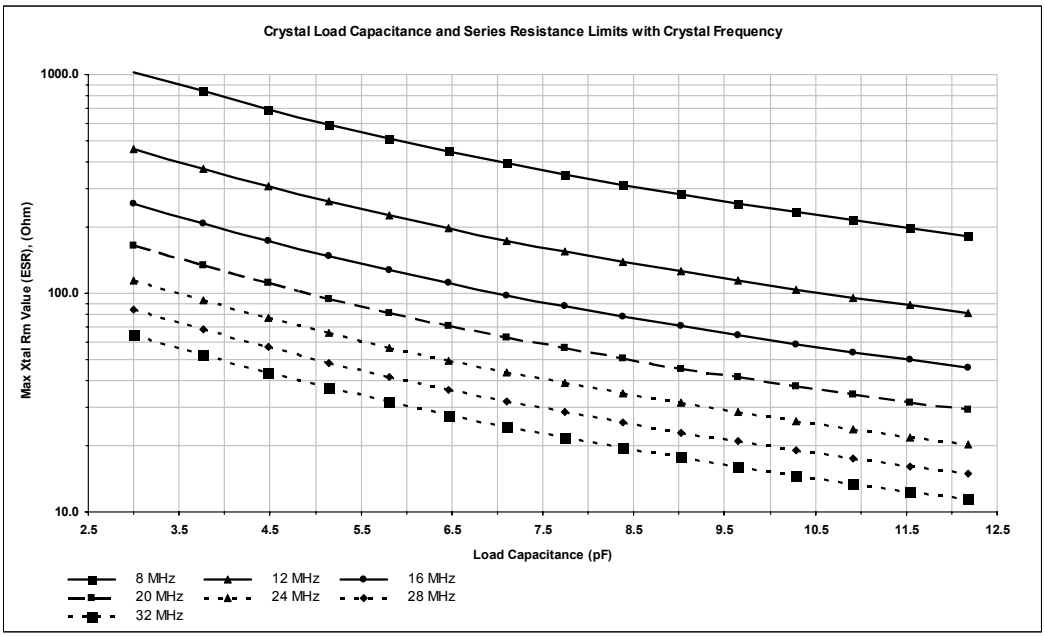


Figure 11.6: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore4-Flash Plug-n-Go crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

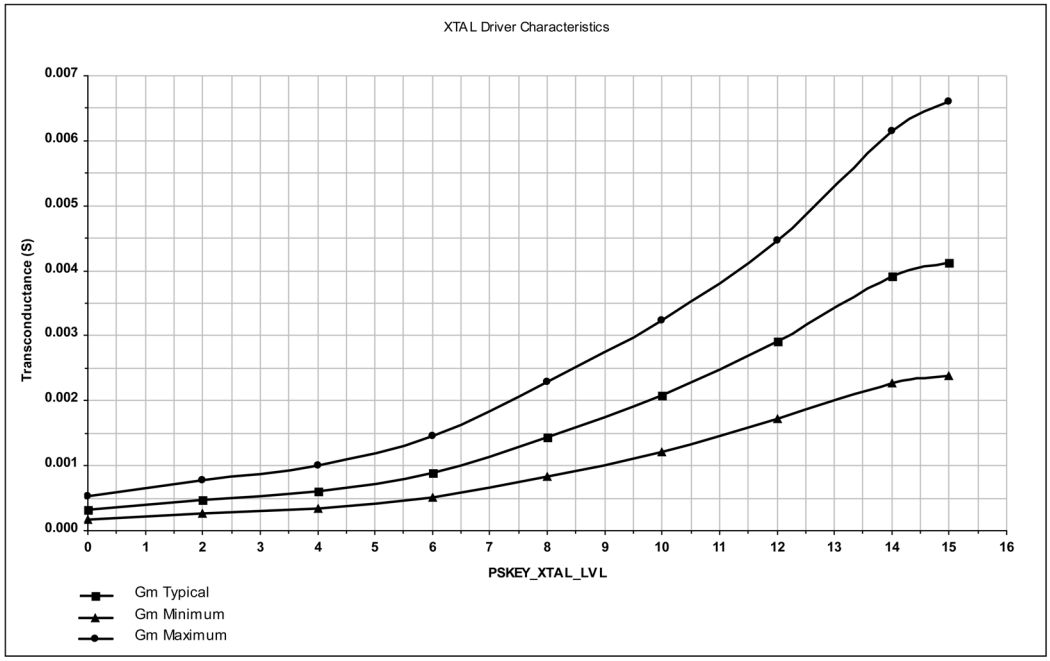


Figure 11.7: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by PS Key PSKEY_XTAL_LVL (0x241).

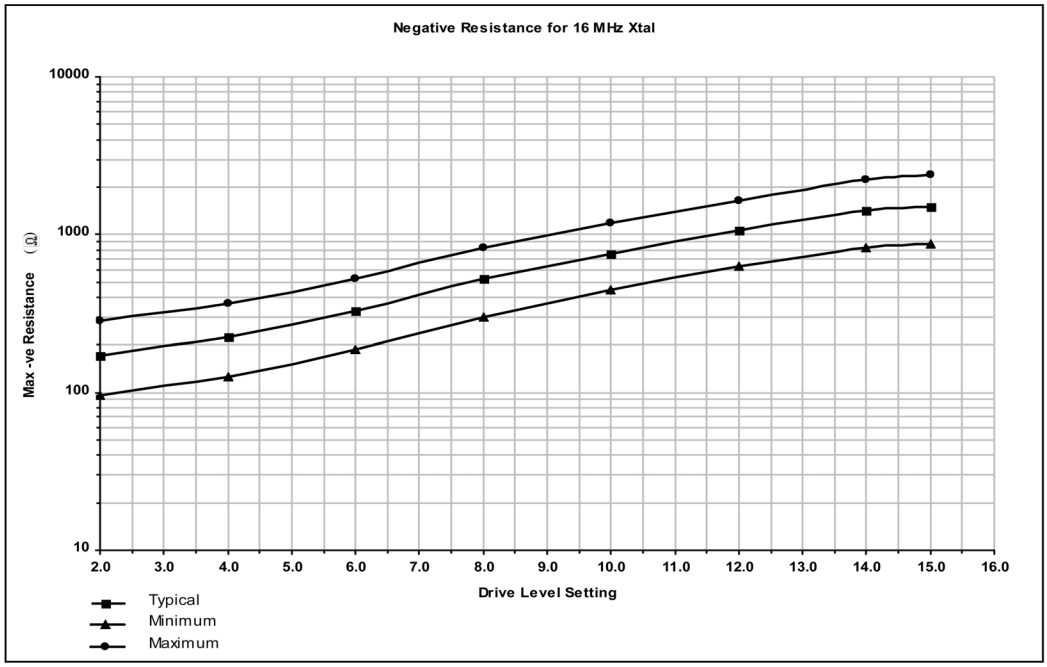


Figure 11.8: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (refer to your software build release note for supported frequencies).

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

11.4 UART Interface

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

BlueCore4-Flash Plug-n-Go UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.(1)

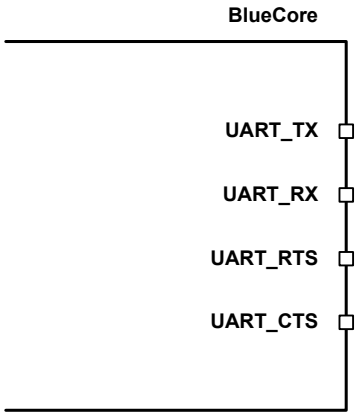


Figure 11.9: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 11.9. When BlueCore4-Flash Plug-n-Go is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore4-Flash Plug-n-Go software.

Note:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		**Possible Values**
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	3M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Channel		8

Table 11.4: Possible UART Settings

The UART interface is capable of resetting BlueCore4-Flash Plug-n-Go upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 11.10. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore4-Flash Plug-n-Go can emit a break character that may be used to wake the host.

(1) Uses RS232 protocol, but voltage levels are 0V to VDD_USB (requires external RS232 transceiver chip).

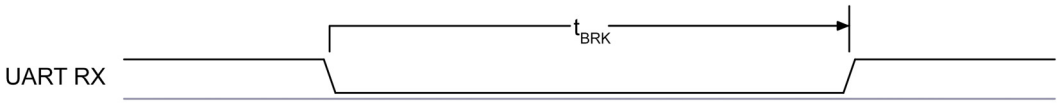


Figure 11.10: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 11.5 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 11.7.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Equation 11.7: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%

Table 11.5: Standard Baud Rates

11.4.1 UART Bypass

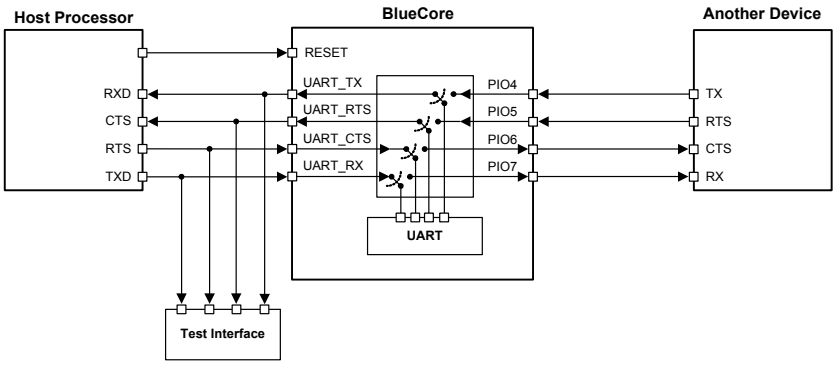


Figure 11.11: UART Bypass Architecture

11.4.2 UART Configuration While RESET is Active

The UART interface for BlueCore4-Flash Plug-n-Go while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore4-Flash Plug-n-Go reset is de-asserted and the firmware begins to run.

11.4.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore4-Flash Plug-n-Go can be used. The default state of BlueCore4-Flash Plug-n-Go after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore4-Flash Plug-n-Go UART, thereby allowing communication to BlueCore4-Flash Plug-n-Go via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.(1)

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore4-Flash Plug-n-Go. Upon this issue, it will switch the bypass to PIO[7:4] as Figure 11.11 indicates. Once the bypass mode has been invoked, BlueCore4-Flash Plug-n-Go will enter the Deep Sleep state indefinitely.

In order to re-establish communication with BlueCore4-Flash Plug-n-Go, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

11.4.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

(1) The range of the signalling level for the standard UART described in section 11.4 and the UART bypass may differ between CSR BlueCore devices, as the power supply configurations are chip dependent. For BlueCore4-Flash Plug-n-Go, the standard UART is supplied by VDD_USB, so has signalling levels of 0V and VDD_USB. Whereas in the UART bypass mode, the signals appear on PIO[4:7] which are supplied by VDD_PADS, therefore the signalling levels are 0V and VDD_PADS.

11.5 USB Interface

This is a full speed (12Mbits/s) Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore4-Flash Plug-n-Go acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a master/slave oriented system (in common with other USB peripherals), BlueCore4-Flash Plug-n-Go only supports USB Slave operation.

11.5.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4-Flash Plug-n-Go, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

11.5.2 USB Pull-Up Resistor

BlueCore4-Flash Plug-n-Go features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4-Flash Plug-n-Go is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

11.5.3 USB Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

11.5.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore4-Flash Plug-n-Go via a resistor network (R_{vb1} and R_{vb2}), so BlueCore4-Flash Plug-n-Go can detect when VBUS is powered up. BlueCore4-Flash Plug-n-Go will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5KΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in BlueCore is only suitable for bus-powered USB devices, e.g., dongles.

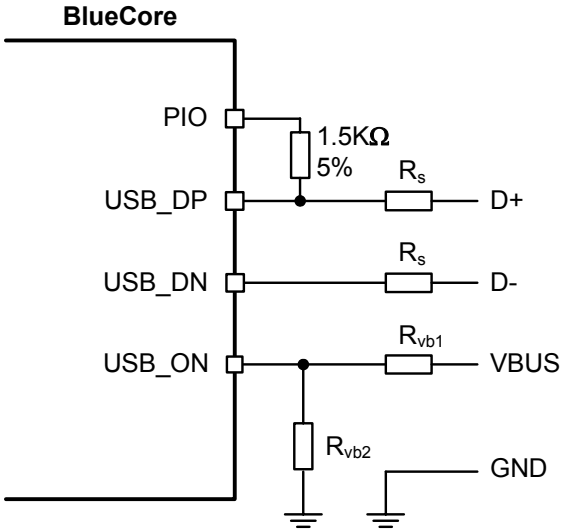


Figure 11.12: USB Connections for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Note:

USB_ON is shared with BlueCore4-Flash Plug-n-Go PIO terminals.

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 11.6: USB Interface Component Values

11.5.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore4-Flash Plug-n-Go negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore4-Flash Plug-n-Go requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10μF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore4-Flash Plug-n-Go will result in reduced receive sensitivity and a distorted RF transmit signal.

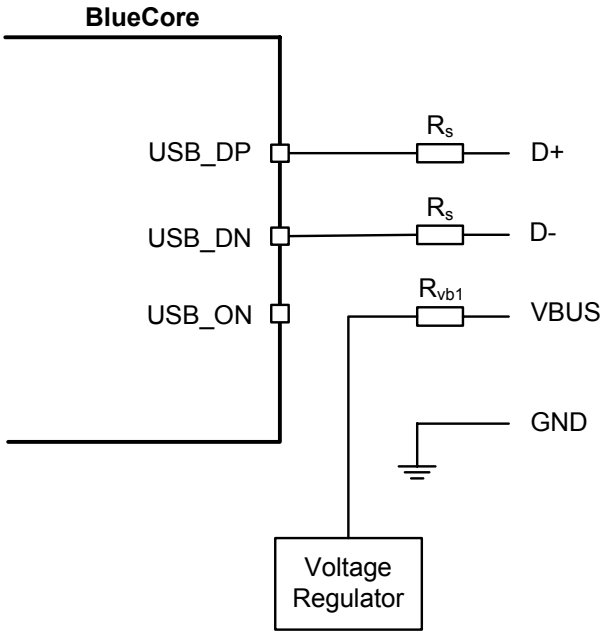


Figure 11.13: USB Connections for Bus-Powered Mode

11.5.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 0.5mA from USB VBUS (self-powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore4-Flash Plug-n-Go. The entire circuit must be able to enter the suspend mode. Refer to separate CSR documentation for more details on USB Suspend.

11.5.7 Detach and Wake_Up Signalling

BlueCore4-Flash Plug-n-Go can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4-Flash Plug-n-Go into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore4-Flash Plug-n-Go to put USB_DN and USB_DP in a high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4-Flash Plug-n-Go will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable) and cannot be sent while BlueCore4-Flash Plug-n-Go is effectively disconnected from the bus.

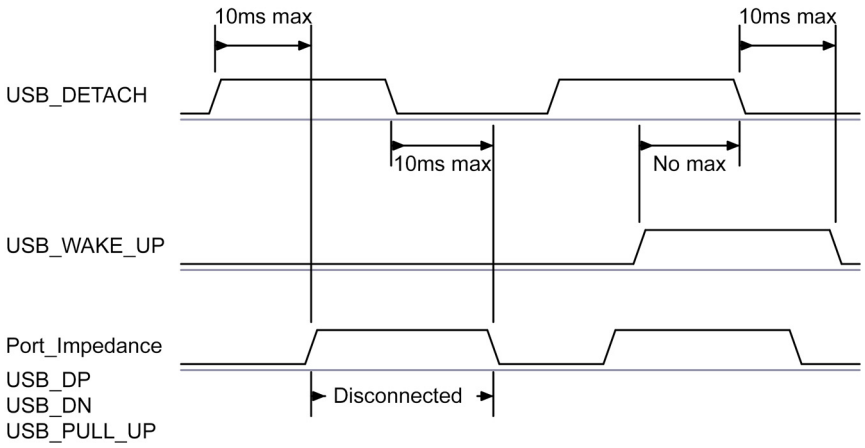


Figure 11.14: USB_DETACH and USB_WAKE_UP Signal

11.5.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4-Flash Plug-n-Go and Bluetooth software running on the host computer. Suitable drivers are available from http://www.csrsupport.com.

11.5.9 USB 1.1 Compliance

BlueCore4-Flash Plug-n-Go is qualified to the USB Specification v1.1, details of which are available from www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore4-Flash Plug-n-Go meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification v2.0 (Chapter 7) electrical requirements.

11.5.10 USB 2.0 Compatibility

BlueCore4-Flash Plug-n-Go is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

11.6 Serial Peripheral Interface

BlueCore4-Flash Plug-n-Go uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore4-Flash Plug-n-Go via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

11.6.1 Instruction Cycle

The BlueCore4-Flash Plug-n-Go is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 11.7: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-Flash Plug-n-Go on the rising edge of the clock line SPI_CLK. When reading, BlueCore4-Flash Plug-n-Go will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is teminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4-Flash Plug-n-Go offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

11.6.2 Writing to the Device

To write to BlueCore4-Flash Plug-n-Go, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

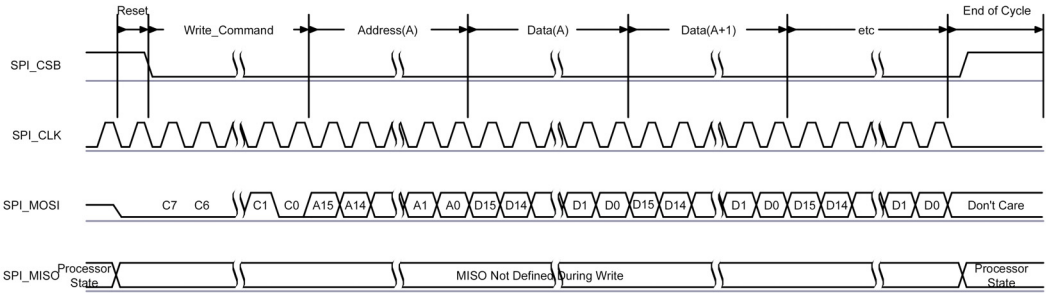


Figure 11.15: SPI Write Operation

11.6.3 Reading from the Device

Reading from BlueCore4-Flash Plug-n-Go is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore4-Flash Plug-n-Go then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

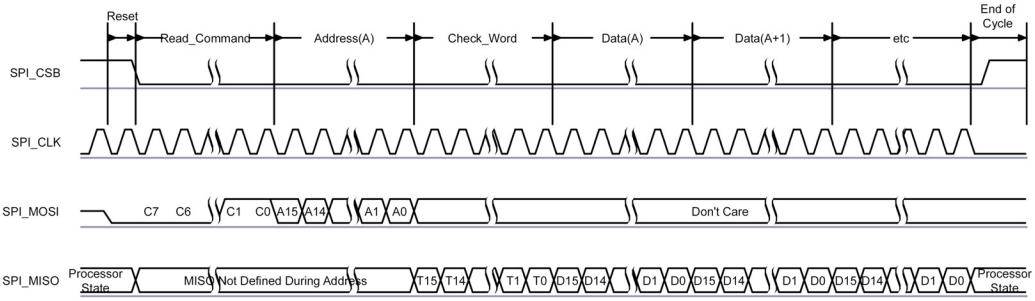


Figure 11.16: SPI Read Operation

11.6.4 Multi-Slave Operation

BlueCore4-Flash Plug-n-Go should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-Flash Plug-n-Go is deselected (SPI_CSB = 1), the SPI_MISO line does not float. Instead, BlueCore4-Flash Plug-n-Go outputs 0 if the processor is running or 1 if it is stopped.

11.7 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore4-Flash Plug-n-Go has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore4-Flash Plug-n-Go offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-Flash Plug-n-Go allows the data to be sent to and received from a SCO connection. (1)

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore4-Flash Plug-n-Go can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. BlueCore4-Flash Plug-n-Go is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

BlueCore4-Flash Plug-n-Go interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-Flash Plug-n-Go is also compatible with the Motorola SSI interface

11.7.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore4-Flash Plug-n-Go generates PCM_CLK and PCM_SYNC.

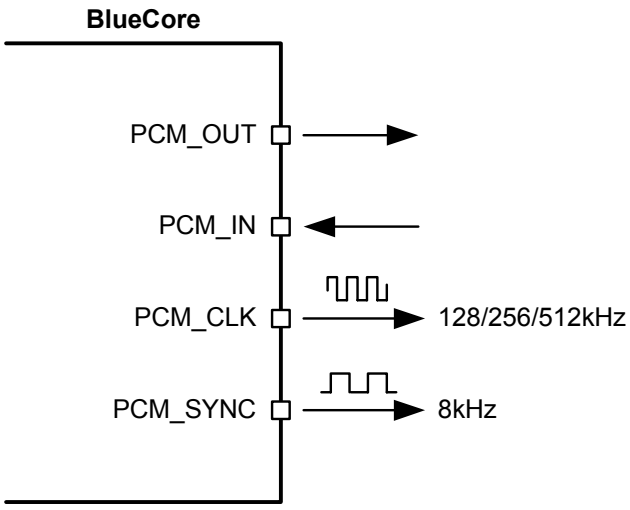


Figure 11.17: BlueCore4-Flash Plug-n-Go as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore4-Flash Plug-n-Go accepts PCM_CLK rates up to 2048kHz.

(1) Subject to firmware support. Contact CSR for current status.

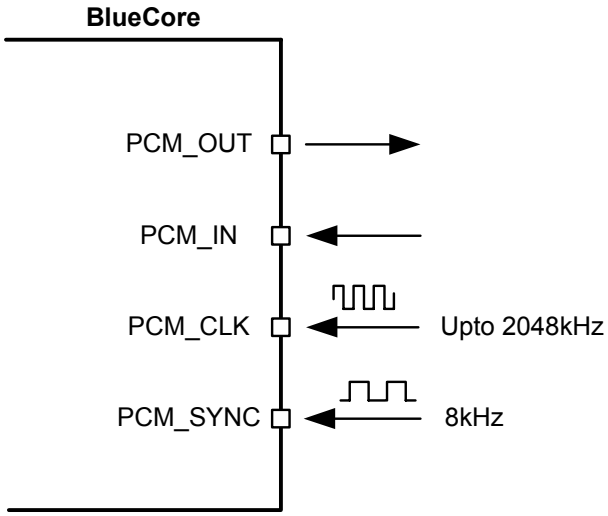


Figure 11.18: BlueCore4-Flash Plug-n-Go as PCM Interface Slave

11.7.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-Flash Plug-n-Go is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-Flash Plug-n-Go is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

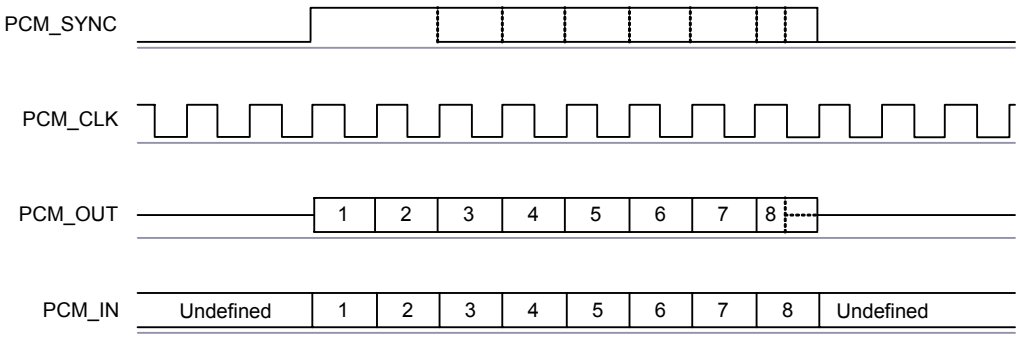


Figure 11.19: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-Flash Plug-n-Go samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

11.7.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

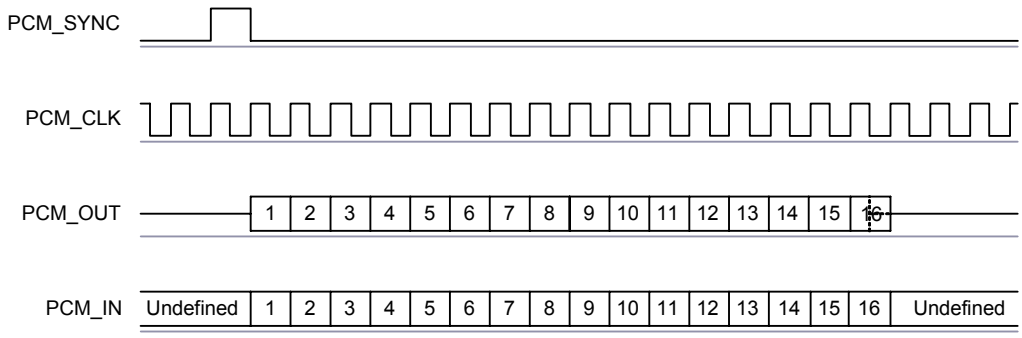


Figure 11.20: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-Flash Plug-n-Go samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

11.7.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

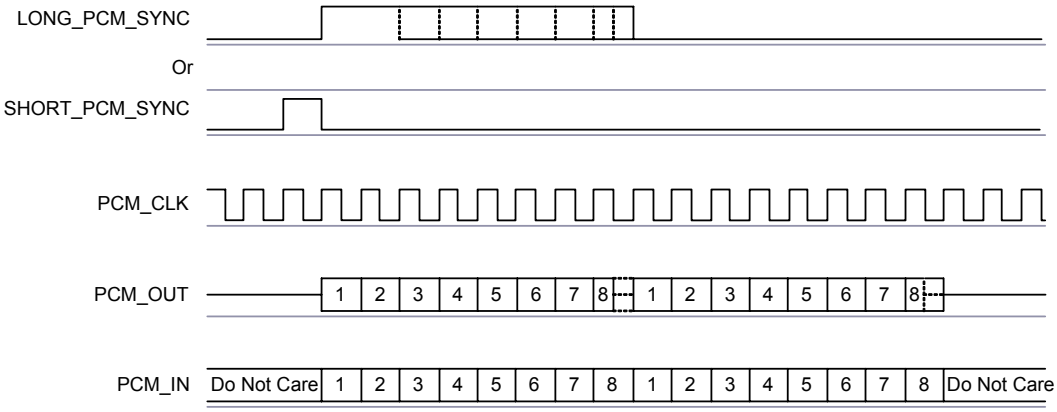


Figure 11.21: Multi-slot Operation with Two Slots and 8-bit Companded Samples

11.7.5 GCI Interface

BlueCore4-Flash Plug-n-Go is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

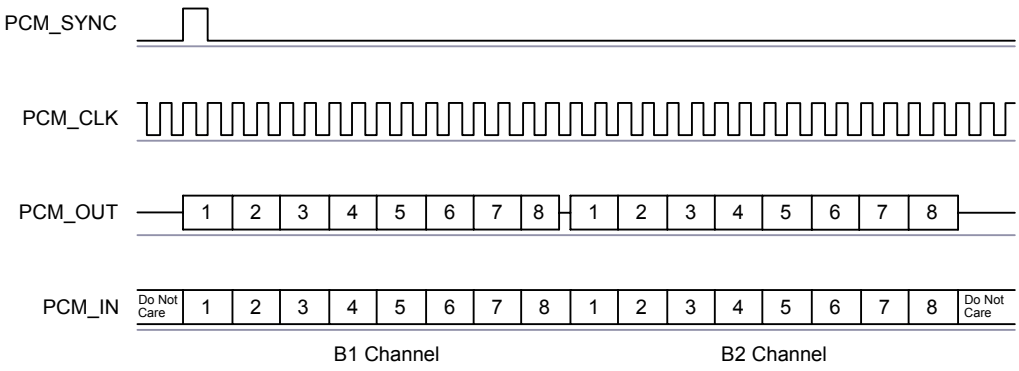


Figure 11.22: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4-Flash Plug-n-Go in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

11.7.6 Slots and Sample Formats

BlueCore4-Flash Plug-n-Go can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore4-Flash Plug-n-Go supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

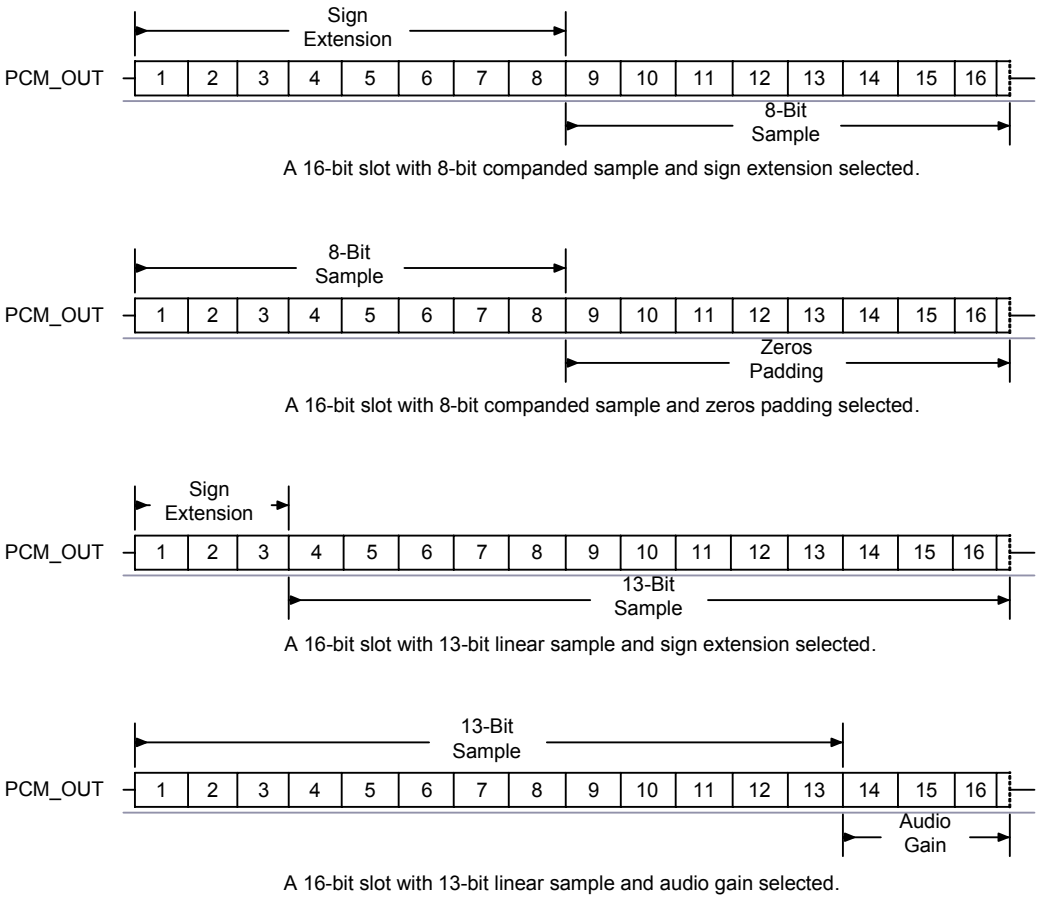


Figure 11.23: 16-Bit Slot Length and Sample Formats

11.7.7 Additional Features

BlueCore4-Flash Plug-n-Go has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

11.7.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 11.10.	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable. See Table 11.11 and PCM_CLK and PCM_SYNC Generation on page 76.	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh}[(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl}[(a)]	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 11.8: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

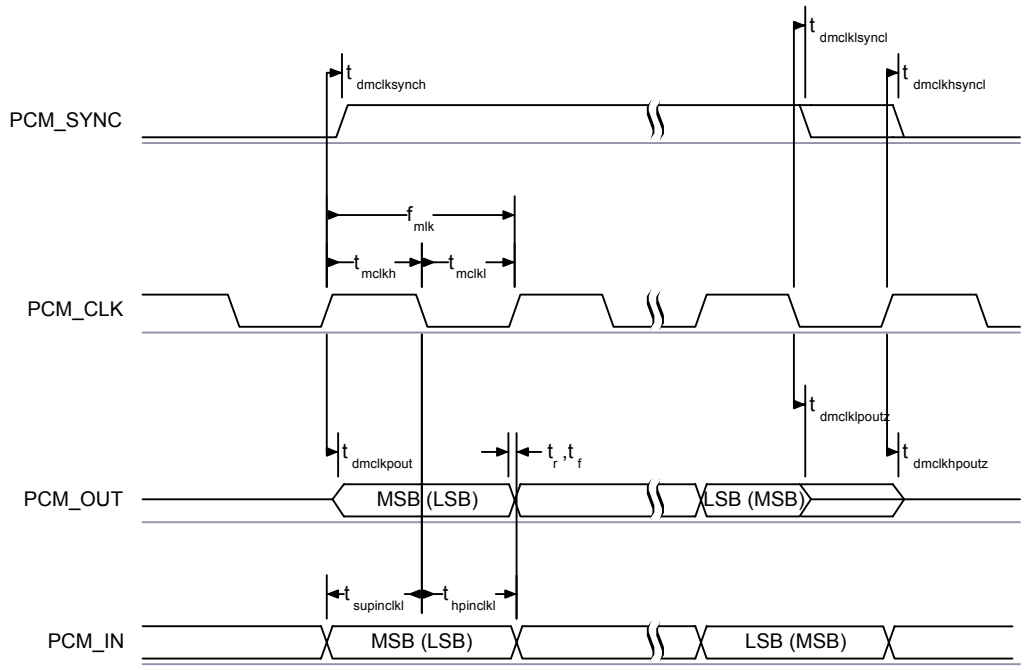


Figure 11.24: PCM Master Timing Long Frame Sync

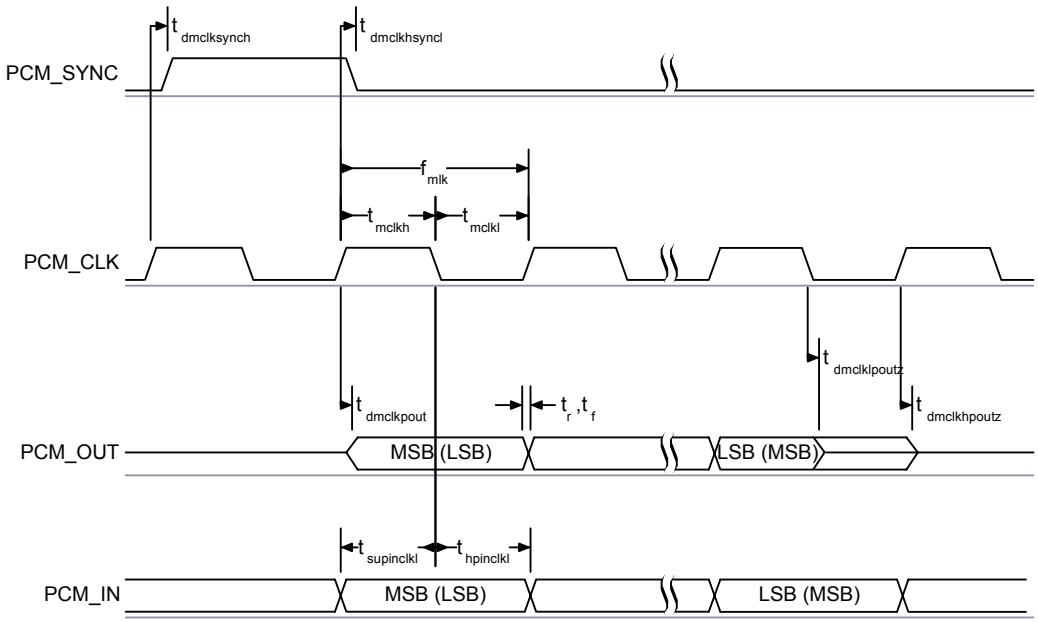


Figure 11.25: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 11.9: PCM Slave Timing

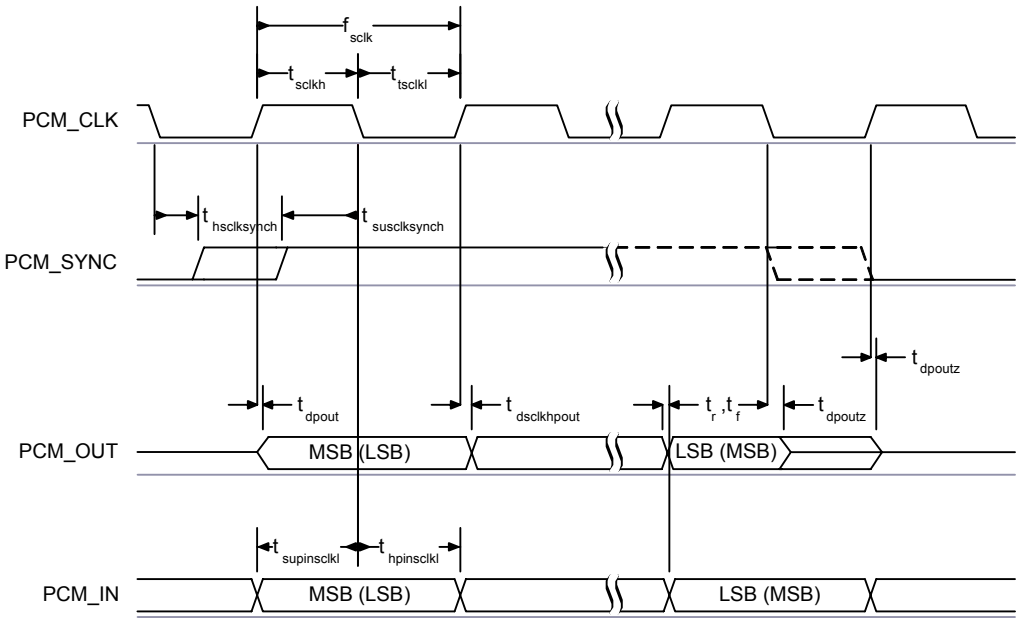


Figure 11.26: PCM Slave Timing Long Frame Sync

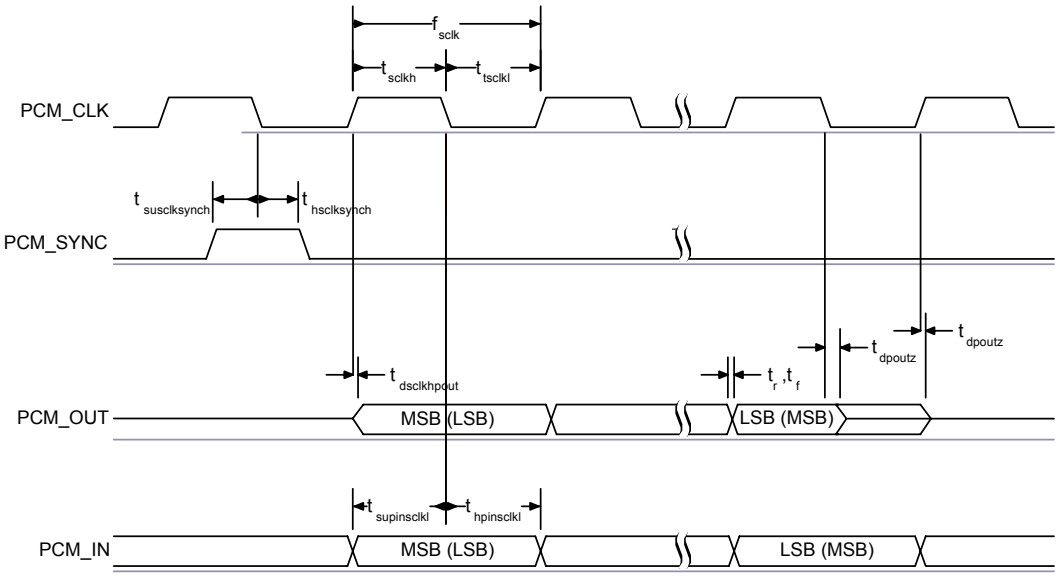


Figure 11.27: PCM Slave Timing Short Frame Sync

PCM_CLK and PCM_SYNC Generation

BlueCore4-Flash Plug-n-Go has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore4-Flash Plug-n-Go internal 4MHz clock (which is used in BlueCore2-External). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

The Equation 11.8 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 11.8: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using Equation 11.9:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 11.9: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

11.7.9 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 detailed in Table 11.10 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 11.11. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

Name	Bit Position	Description
-	0	Set to 0
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode
MUTE_EN	10	1 = force PCM_OUT to 0
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.

Name	Bit Position	Description
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 11.10: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 11.11: PSKEY_PCM_LOW_JITTER_CONFIG Description

11.8 I/O Parallel Ports

Fifteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_MEM.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore4-Flash Plug-n-Go is provided from a system application specific integrated circuit (ASIC). Using PSKEY_CLOCK_REQUEST_ENABLE (0x246), this terminal can be configured to be low when BlueCore4-Flash Plug-n-Go is in Deep Sleep and high when a clock is required. The clock must be supplied within 4ms of the rising edge of PIO[6] or PIO[2] to avoid losing timing accuracy in certain Bluetooth operating modes.

BlueCore4-Flash Plug-n-Go has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2] also known as the extended PIO lines. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage; the other two may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals: 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals, the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (e.g., clocks), the output voltage level is determined by VDD_MEM (1.8V).

11.8.1 PIO Defaults

CSR cannot guarantee that these terminal functions remain the same. Refer to the software release note for the implementation of these PIO lines, as they are firmware build-specific.

11.9 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-Flash Plug-n-Go where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-Flash Plug-n-Go.

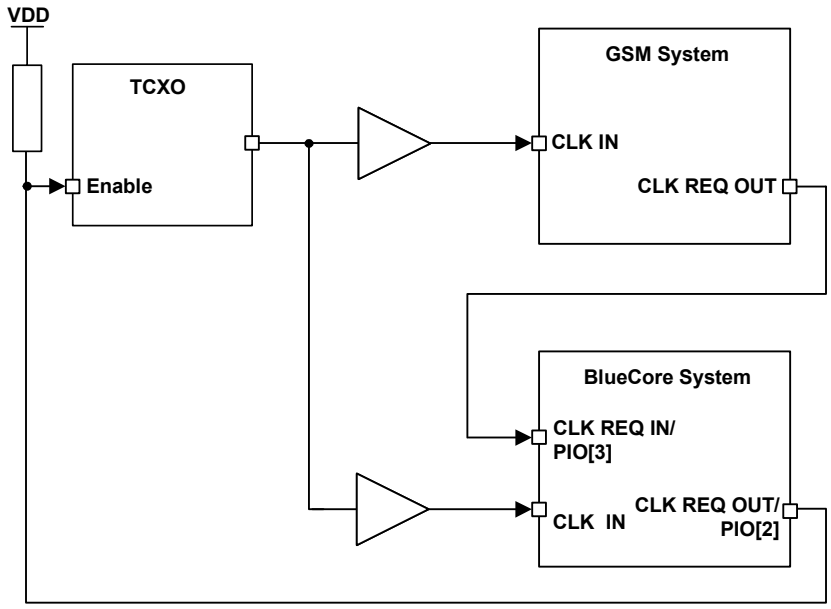


Figure 11.28: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

11.10 RESET and RESETB

BlueCore4-Flash Plug-n-Go may be reset from several sources:

- RESET or RESETB pins
- Power on reset
- A UART break character
- Via a software configured watchdog timer

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5ms and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is OR'd on-chip with the active high RESET, with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-downs.

Following a reset, BlueCore4-Flash Plug-n-Go assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-Flash Plug-n-Go is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-Flash Plug-n-Go free runs, again at a safe frequency.

11.10.1 Pin States on Reset

Table 11.12 shows the pin states of BlueCore4-Flash Plug-n-Go on reset.

Pin Name	State: BlueCore4-Flash Plug-n-Go
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-state with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-state with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-state with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-state with weak pull-down
AIO[2:0]	Output, driving low
RESET	Input with weak pull-down
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
AUX_DAC	High impedance
RF_IN	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 11.12: Pin States of BlueCore4-Flash Plug-n-Go on Reset

11.10.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset[1] : Baud rate and RAM data not available

(1) A Cold Reset is either Power cycle, system reset (firmware fault code) or Reset signal. See section 11.10.

11.11 Power Supply

11.11.1 Voltage Regulator (Plug-n-Go)

An on-chip linear voltage regulator can be used to power the 1.8V dependent supplies. It is advised that a smoothing circuit using a 2.2µF low ESR capacitor and 2.2Ω resistor be placed on the output VDD_ANA.

In the Plug-n-Go package, an internal 2.2Ω resistor is provided between the regulator output VDD_ANA and VDD_DIG.

The regulator is switched into a low power mode when the device is sent into Deep Sleep mode. When the on-chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

11.11.2 Sequencing

It is recommended that VDD_CORE, VDD_RADIO and VDD_ANA be powered at the same time. The order of powering supplies for VDD_CORE, VDD_PIO, VDD_PADS and VDD_USB is not important. However, if VDD_CORE is not present, all inputs have a weak pull-down irrespective of the reset state.

11.11.3 Sensitivity to Disturbances

CSR recommends if supplying BlueCore4-Flash Plug-n-Go from an external voltage source that VDD_ANA and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. In addition, avoid single tone frequencies. CSR recommends a simple RC filter for VDD_CORE, as this reduces transients put back onto the power supply rails.

The remaining supplies VDD_PIO, VDD_PADS and VDD_USB can be connected together with the VREG_IN to the 3.3V supply and simply decoupled.

The transient response of the regulator is also important. At the start of a packet, power consumption will jump to high levels. See the average current consumption section. The regulator should have a response time of 20µs or less; it is essential that the power rail recovers quickly.

11.11.4 VREG_EN Pin

The regulator enable pin, VREG_EN, can be used to enable and disable the BlueCore4-Flash Plug-n-Go device if the on-chip regulator is being used. The pin is active high and has an internal weak pull-up to enable the regulator if VREG_EN is not connected.

12 Product Reliability Tests

Die	Test Conditions	Specification	Sample Size
ESD	Human Body Model	JEDEC	36
Latch-up	±200mA	JEDEC	6
Early Life	125°C	48 – 168 hours	240
Hot Life Test	125°C	1000 hours	320 (240 FITs)

Package	Test Conditions	Specification	Sample Size
Moisture Sensitivity Precon JEDEC Level 3	(125°C 24 hours) 30°C/60%RH	192 hours five re-flow simulation cycles	308
Temperature Cycling	-65°C to +150°C	500 cycles	77
AutoClave (Steam)	121°C at 100% RH	96 hours	77
HAST	130°C/85% RH	96 hours	77
Thermal Shock	-55/125°C	100 cycles	77
High Temperature Storage	150°C	1000 hours	77

13 Product Reliability Tests for BlueCore4-Flash Plug-n-Go Automotive

13.1 AEC-Q100

The reliability tests in this section follow the tests outlined in the AEC-Q100 and were performed on BlueCore4-Flash Plug-n-Go in VFBGA 10 x 10mm 96 I/O (lead-free solder balls). Samples are electrically tested at ambient temperature.

This package qualification will (where moisture sensitivity preconditioning is required) use IPC/Jedec MSL3, i.e., the finished product is allowed a maximum exposure to a ≤30°C/60%RH environment for 168 hours before mounting.

As part of CSR's automotive test program, customers will have access to the initial device reliability test report. They will also have access to a quarterly reliability test report update for automotive parts.

Die	Test Conditions	Specification	Sample Size
ESD	Human Body Model	JEDEC	24
Early Life	125°C VDD_{max}	48 hours	2400
Hot Life Test	125°C VDD_{max}	1000 hours	90, 77, 77

Package	Test Conditions	Specification	Sample Size
Moisture Sensitivity Precon JEDEC Level 3	(125°C 24 hours) 30°C/60%RH	192 hours five reflow simulation cycles	783
Temperature Cycling	-65/150°C	500 cycles	231 from Precon
Autoclave (Steam)	121°C/100%RH	96 hours	231 from Precon
Temperature Humidity Bias	85°C/85%RH Vdd_{max}	1000 hours	231 from Precon
Thermal Shock	-55/125°C	100 cycles	77 from Precon
High Temperature Storage	150°C	1000 hours	77

Other	Test Conditions	Sample Size
Bond Shear	Acid decapsulation of finished product	30 bonds
Wire Pull	Acid decapsulation of finished product	60 wires from Precon and temperature cycling
Solder Ball Shear	Two reflow cycles	150 balls
Visual Inspection and Dimensions	N/A	30 devices

14 Application Schematic

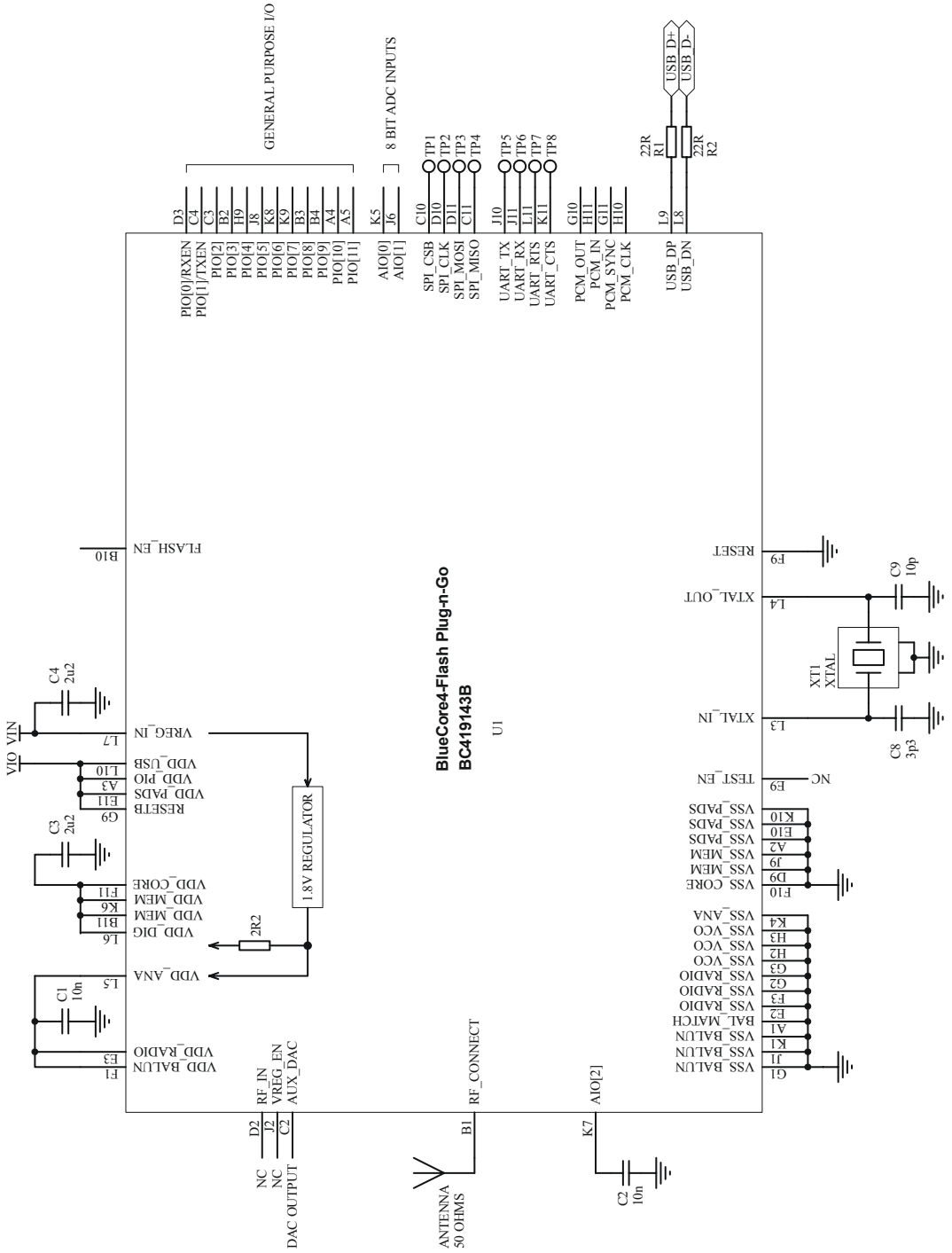
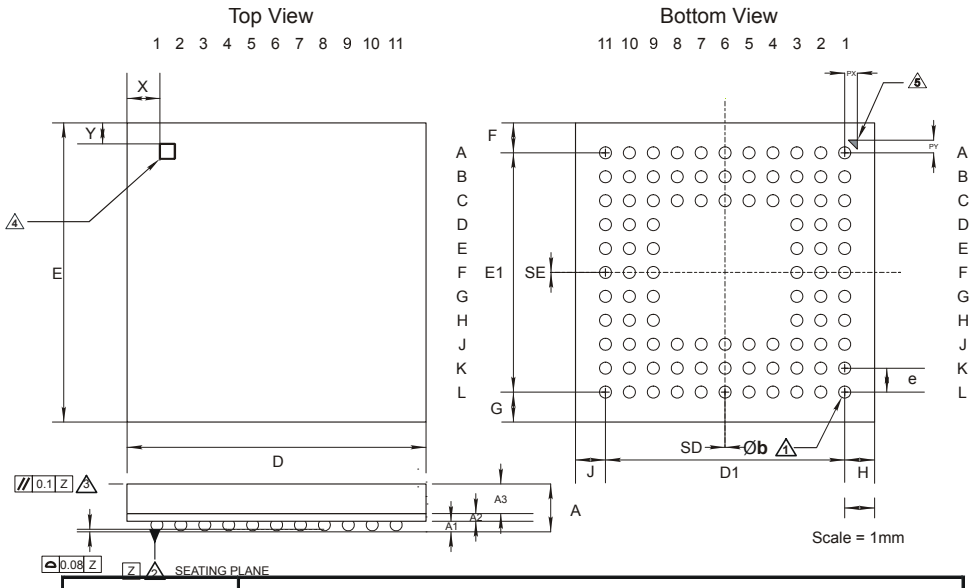


Figure 14.1: Application Circuit for Radio Characteristics Specification

15 Package Dimensions

15.1 10 x 10 LFBGA 96-Ball 1.6mm Package



Description	96-Ball Low-Profile Fine-Pitch Ball Grid Array (LFBGA)			
Size	10 x 10 x 1.6mm			
Pitch	0.8mm			
Package Ball Land	Solder mask defined. Solder mask aperture 300µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A			1.6	(1) Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.30	0.35	0.40	
A2		0.26		
A3		0.80		(2) Datum Z is defined by the spherical crowns of the solder balls
b	0.35	0.40	0.45	
D	9.90	10.00	10.10	(3) Parallelism measurement shall exclude any effect of mark on top surface of package
E	9.90	10.00	10.10	
e		0.80		
D1		8.00		(4) Top-side polarity mark. The dimensions of the square polarity mark are 0.5 x 0.5mm.
E1		8.00		
F	0.950	1.000	1.050	(5) TBA Bottom-side polarity mark. The dimensions of the triangular polarity mark are 0.30 x 0.30 x 0.42mm.
G	0.950	1.000	1.050	
H	0.950	1.000	1.050	
J	0.950	1.000	1.050	
PD		0.300		
PX		0.420		
PE		0.300		
PY		0.420		
SD		0		
SE		0		
X		1.10		
Y		0.70		
JEDEC	MO-210			
Unit	mm			

Figure 15.1: BlueCore4-Flash Plug-n-Go 96-Ball LFBGA 1.6mm Package Dimensions

16 RoHS Statement with a List of Banned Materials

16.1 RoHS Statement

BlueCore4-Flash Plug-n-Go where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

16.1.1 List of Banned Materials

The following banned substances are not present in BlueCore4-Flash Plug-n-Go which is compliant with RoHS:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- PBB (Polybrominated Bi-Phenyl)
- PBDE (Polybrominated Diphenyl Ether)

In addition, BlueCore4-Flash Plug-n-Go is free from the following substances:

- PVC (Poly Vinyl Chloride)

17 Ordering Information

17.1 BlueCore4-Flash Plug-n-Go

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	96-Ball LFBGA (Pb free)	10 x 10 x 1.6mm	Tape and reel	BC419143B-ANN-E4 [a]

[a] Until BlueCore4-Flash Plug-n-Go reaches **Production** status order number is BC419143BES-ANN-E4.

Minimum Order Quantity

2kpcs taped and reeled

18 Contact Information

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19 Document References

Document:	Reference
Specification of the Bluetooth system	v1.1, 22 February 2001 and v1.2, 05 November 2003
Bluetooth Core Specification v2.0 + EDR	v2.0+EDR, 8 November 2004
Bluetooth Test Document v2.0+EDR	v2.0.e.0, 5 November 2004
Universal Serial Bus Specification	v1.1, 23 September 1998
Selection of Flash Memory for Use with BlueCore	CSR document bcore-an-001P
Selection of I^2C EEPROMS for Use with BlueCore	CSR document bcore-an-008P
IA-481-2	16mm, 24mm, 32mm, 44mm and 56mm Embossed Carrier Taping of Surface Mount Components for Automatic Handling
EIA-541	Packaging Material Standards for ESD Sensitive Items
EIA-583	Packaging Material Standards for Electrostatic Discharge (ESD) Sensitive Items
IPC / JEDEC J-STD-033	Standard for Handling, Packing, Shipping and Use of Moisture / Reflow Sensitive Surface Mount Devices

20 Terms and Definitions

8DPSK	8 phase Differential Phase Shift Keying
π/4 DQPSK	pi/4 rotated Differential Quaternary Phase Shift Keying
BlueCore®	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. Bluetooth data packet
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
A-law	Audio encoding standard
ALU	Arithmetic Logic Unit
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BMC	Burst Mode Controller
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CRC	Cyclic Redundancy Check
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DDS	Direct Digital Synthesis
DC	Direct Current
DFU	Device Firmware Upgrade
DNL	Differential Linearity Error
DSP	Digital Signal Processor
EDR	Enhanced Data Rate
eSCO	Extended SCO
ESR	Equivalent Series Resistance
FIR	Finite Impulse Response
FSK	Frequency Shift Keying

GCI	General Circuit Interface
GFSK	Gaussian Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
I²C™	Inter-Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
INL	Integral Linearity Error
IQ Modulation	In-Phase and Quadrature Modulation
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
Kalimba	DSP core for CSR's range of chips
ksps	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LFBGA	Low profile Fine Ball Grid Array
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LSB	Least-Significant Bit
MCU	MicroController Unit
μ-law	Audio Encoding Standard
MIPS	Million Instructions Per Second
MMU	Memory Management Unit
MISO	Master In Serial Out
NOB	Number Of Bits
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCM	Pulse Code Modulation. Refers to digital voice data
PDA	Personal Digital Assistant
Persistent Store	Storage of BlueCore's configuration values in non-volatile memory
PIO	Parallel Input Output
PICS	Profile Implementation Confirmation Statement
pk-pk	Peak to Peak
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)

REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SINAD	SIgnal to Noise ratio And Distortion
SNR	Signal to Noise Ratio
SPDIF	Sony and Philips Interface Specification
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TBD	To Be Defined
TCXO	Temperature Controlled crystal Oscillator
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UHCI	Upper Host Control Interface
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)

21 Document History

Date	Revision	Reason for Change
FEB 05	a	Original publication of this document. (CSR reference: BC419143B-ds-001Pa)
MAR 05	b	Amended System Architecture and Device Diagrams. Added Balun and Filter block description. Minor amends. (CSR reference: BC419143B-ds-001Pb)
APR 05	c	Amended maximum baud rate to 3M baud and added additional data rates.
JUL 05	d	Electrical Characteristics and Radio Characteristics - Basic Data Rate updated to reflect a radio performance temperature range of -40°C to +85°C. Updated Auxilliary DAC in Description of Functional Blocks Amendment to note (a) concerning specified output voltage in the Auxilliary DAC table (Input/Output Terminal Characteristics) in Electrical Characteristics. Amendment to note (g) concerning VREG_EN and VREG_IN in Linear Regulator table in Electrical Characteristics. Power Consumption moved from Radio Characteristics to Electrical Characteristics section. Changed title of Record of Changes to Document History; changed title of Acronyms and Abbreviations to Terms and Definitions.
APR 06	e	Updated references to VDD_MEM. See Electrical Characteristics, and Sensitivity to Disturbances in Device Terminal Descriptions.

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